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Evaluation of a multiphase cascaded H-bridge inverter for induction motor operation

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Multi-phase systems are becoming more popular for applications requiring high power and precise motor control, even if single-phase AC power is still frequently utilized in households and some enterprises. While both systems have benefits over single-phase, there are trade-offs associated with each. Because of its balanced operation and effective power transfer, the three-phase (3-Φ) system is the most widely used multi-phase system. Nevertheless, different phase values can be investigated for particular applications where reducing torque ripple and harmonic content is essential. Using odd numbers of phases (such as 5-Φ) that are not multiples of three is one method. This design has the ability to reduce torque ripple by producing a more balanced magnetic field as compared with even-numbered phases. But adding more phases also makes the system design and control circuitry more complex. Systems with five phases (5-Φ) provide a compromise between performance and complexity. Applications such as electric ship propulsion, rocket satellites, and traction systems may benefit from their use. Nevertheless, choosing a multi-phase system necessitates carefully weighing the requirements unique to each application, taking into account elements like cost, power transmission, control complexity, and efficiency. The increasing popularity of electric vehicles and renewable energy technologies has led to the need for inverters in current electric applications. Conventional inverters provide square wave outputs, which cause the drive system to become noisy and cause harmonics. Multi-phase multilevel inverters can be used to enhance inverter functioning and produce an improved sinusoidal output. This study focuses on an induction motor drive powered by a five-phase multilevel cascaded H-Bridge inverter. With less torque and current ripples in the motor rotor, the power conversion harmonics are reduced and the switching components of the inverter are under less stress. However, in comparison to traditional inverters, it does require a greater number of legs. Because the switches needed for the cascaded H-Bridge inverter are less expensive in five-phase systems, they are favoured over higher phase orders. Furthermore, the suggested inverter removes 5th order harmonics, something that is not possible with traditional inverters. A five-phase induction motor appropriate for variable speed driving applications is also suggested by this research. Lastly, utilizing pulse width modulation (PWM) converters and an FPGA controller, an experimental study is carried out to assess the dynamic performance of the suggested induction motor drive. Particular attention is paid to the In-Phase Opposition Disposition (IPD) PWM technique.

Keywords Induction motors, Inverters, Motor drives, Modular multilevel converters, Power conversion harmonics, Power semiconductor devices, Pulse width modulation converters, Variable speed drives

Abbreviations

CHB	Cascaded H-bridge
CHBMLI	Cascaded H-bridge multi level inverter
CLB	Configurable logic blocks

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CMV	Common mode voltage
CRO	Cathode ray oscilloscope
DCM	Digital clock managers
DSO	Digital storage oscilloscope
DSP	Digital signal processor
DTC	Direct torque control
EMI	Electro magnetic interferences
FCMLI	Flying capacitor multi level inverter
FCS	Finite control set
FPGA	Field-programmable gate array
FPIM	Five-phase induction motor
FPIMD	Five phase induction motor drive
HCB	Hierarchical control blocks
HDL	Hardware description language
IM	Induction motors
IOBs	Input/output blocks
IPD	In-phase opposition disposition
MFPCC	Model-free predictive current control
MMF	Magnetomotive force
MPC	Model predictive control
NPC/DCMLI	Diode-clamped multilevel inverter
PD	Phase disposition method
PLL	Phase-locked loops
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
RAM	Random access memory
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
VSI	Voltage source inverter
VVB	Voltage vectors

For many years, three-phase induction motors have served as the foundation for industrial applications, providing dependable and effective power to machinery. Nonetheless, multi-phase induction motors and inverters are becoming attractive substitutes for certain requirements requiring even smoother operation, improved fault tolerance, or precise torque control.

- *Lower harmonic content* Compared to a three-phase motor, the stator winding has more phases, which results in a spinning magnetic field with less distortion from the supply current. When a motor operates with less harmonic content, it may become more efficient and produce fewer torque pulsations.
- *Fault tolerance* Multi-phase motors can demonstrate some degree of continuous functioning in the event of a fault, in contrast to three-phase motors, which may undergo total shutdown if one phase opens while the motor is operating. However, it's crucial to remember that in order for a multi-phase motor to continue operating following a phase defect, extra control techniques or fault-tolerant designs could be required.
- *Less torque ripple* When compared with three-phase motors, multi-phase motors may have less torque ripple. Applications like electric vehicle propulsion or robotics that demand extremely smooth and accurate torque control may benefit from this.

It's crucial to keep in mind that although multi-phase systems have these potential advantages, their control circuitry and system architecture become more complex. The particular application requirements, taking into account variables like efficiency, torque ripple reduction needs, fault tolerance requirements, and overall system complexity, will determine whether to use a multi-phase system or a typical three-phase system. While three-phase inverters have dominated power conversion applications, multi-phase inverters are gaining traction due to their potential for improved performance, reliability, and efficiency

- *Harmonic mitigation* By distributing the inherent harmonic content of the power conversion process more equally over a larger number of phases, multi-phase inverters reduce harmonic distortion. As a result, the output waveform has less THD. This is especially advantageous in applications where harmonic distortion must be kept to a minimum in order to avoid interfering with other grid equipment, and where strict power quality requirements apply.
- *Enhanced fault tolerance* Multi-phase inverters can display some fault tolerance, much as their multi-phase motor counterparts. Some designs of multi-phase inverters may be able to function even in the case of a single-phase failure, if at a decreased power output. More fault tolerance leads to more reliable systems, particularly in applications that are vital wherein interruption must be kept to a minimum.
- *Diminished switching losses* Heat and energy losses are produced during the switching process in inverters. When compared to conventional three-phase systems, switching losses from multi-phase inverter designs may be reduced. Longer component lifespans may result from this increased overall efficiency and decreased heat generation within the inverter.

- *Higher power quality* Higher power quality is the result of enhanced fault tolerance and decreased harmonic distortion working together. Thus, there is less chance of malfunctions or damage from power quality problems and linked equipment will have a cleaner, more dependable power source.
- *Adaptability to new uses* Multi-phase inverters' special benefits make them appropriate for a variety of newly developed uses.

The ability of multi-phase induction motors and inverters to solve certain application issues is what drives the adoption of these devices. They are an appealing option for many applications, especially those with strict operating and geographical restrictions, since they have the potential to increase overall efficiency, boost system reliability, and improve performance.

Electrical engineering is being forced to expand in response to the growing need for power in a variety of industries. With clear benefits over conventional single-phase and three-phase systems, multi-phase systems are a potential new technology, especially for applications that demand specialized performance attributes. The capacity of multi-phase systems to produce smoother operation is one of its main advantages. When compared to conventional motors, multi-phase motors show less torque ripple, which lessens mechanical vibrations and may lead to less component wear. This translates to advantages in fields like robots and electric cars that require exact control. In addition, compared to three-phase systems, which usually shut down in similar circumstances, certain multi-phase systems can demonstrate some degree of continuous functioning even with a phase failure, improving overall system reliability. This enhanced fault tolerance is essential for applications where unacceptably long downtime occurs. Multi-phase motors can attain a higher power density than their three-phase counterparts in applications where space is limited. For scenarios where weight and size are constraints, this small design is a big benefit. Furthermore, more degrees of freedom for control techniques are offered by the extra phases in multi-phase systems. Better motor control is made possible by this, which may lower power supply harmonics and increase system efficiency as a whole. Multi-phase systems are the subject of continuing research and development activities with the goal of further optimizing their performance for a wider range of applications. By concentrating on improving multi-phase technology, we may push the boundaries of power electronics and electrical engineering and possibly increase performance and efficiency across a range of industries.

In the field of drives and all other necessary requirements, multiphase supply is used extremely frequently. Thyristor-based inverters are used for high power applications, while gate-controlled turn-off devices like power BJTs, MOSFETs, IGBTs, GTOs, SITs, etc. are used in low and medium power inverters. Advanced power semiconductor devices like IGBTs are preferably used for high power handling capabilities, which are generally used for the inverter. In order to control the magnitude and frequency, inverters are operated with switched mode power supplies. IGBTs are commonly used in the power electronic circuits of multi-phase inverters due to their ability to handle high voltage and current levels. These are crucial for controlling the flow of power in the inverter, enabling the conversion of DC to AC in multi-phase systems.

In multi-phase inverter systems IGBTs are a common option for switching components. These provide an advantageous compromise between the rapid switching speed of MOSFETs and the ability of several high-voltage power semiconductor devices, including but not limited to conventional BJTs, to handle voltage.

A multi-phase inverter's best device selection is based on a number of application-specific variables, including: IGBTs can function at frequencies that are typically enough for the majority of multi-phase inverter applications, and higher switching frequencies can be advantageous for certain applications. The voltage rating required for the selected device will depend on the particular voltage requirements of the application. IGBTs can be found in a variety of voltage levels to suit a variety of applications. When choosing a device, a number of considerations must be taken into account, including switching speed, conduction losses, and overall system efficiency. IGBTs are a strong option for numerous multi-phase inverter applications because they provide a decent balance in these areas.

In industrialized application, for a ample range of speed control Voltage source inverters are preferred. In VSI, the output depends on the input dc voltage. As per load requirements, that means if the load requires fixed ac then the inverter should have the capability of delivering, even though the given input has certain variations. Here that the voltage control is necessary to reimburse the variations in the dc input. *V/f* ratio maintained as constant, to control the induction motor (IM). Usually voltage control is important to regulate the load variations.

In earlier day's high power rating with limited voltage obtained by multi-level inverter-fed ac machine drives. But, at present to attain high power ratings, low rated current devices are utilized with the advancement of power electronic apparatus in addition to multiphase machine drives. In a squirrel cage IM, the rotor bars are short circuited and the stator is activated by source voltage. As a result, the supply voltage can be increased proportionally to the stator side's phase count. By using modular MULTI LEVEL converters, which have more phases and levels than standard inverters, these issues are solved. Using PWM at a high switching frequency, a multi-level converter is used to power a FPIM. Torque fluctuations grow as frequency rises, however the intensity of the fluctuation can be lessened by raising the motor's phase count. V/f speed control approach is proposed for the motor drive. This FPIMD is more dependable than traditional drives and has a high energy efficiency.

Related work

Earlier the research was very sluggish on multi-phase systems, but due to rapid growth in power semiconductor devices, numerous research work has been carried out by various authors on multi-phase drives. The proposed work is consolidated after understanding the integral conceptual solutions on the multi-phase drives. The proposed drives' control strategies include DTC, vector control, and space vector PWM. When compared to the traditional 3-φ motor drives, the pros and cons are described in[1]. The researcher used collective formation to analyze the proposed drive's dynamic performance. Third harmonic inoculation is a new technique[2] for adjustable speed

drives that have more phases than traditional speed drives. To improve the drive's performance in comparison to other speed drives currently on the market, current harmonics are added to the motor's concentric windings. The MMF is distributed sinusoidally in the windings of the proposed drive in Multiphase IM Drives with Synchronous Current Control Scheme[3]. Current controllers are typically thought of in synchronous reference frames, although this has certain drawbacks. In order to get over these restrictions, traditional controllers are adjusted, which removes the imbalances in the suggested drive and makes it run smoothly under any circumstances. In order to analyze the RMS current ripples of the drive, multiphase IM drives are used using different connection schemes of the polygon access and pulse width modulation techniques[4].

For the variable speed of 5-φ IM using vector control with model reference adaptive control[5] is derived from the basic predictive control. This technique is successfully implemented for the conventional drives. By creating the 6-φ IM dynamic model, a new multiphase induction motor model was created[6]. Three-phase stator winding and three-phase rotor winding are in synchronization. The characteristics such as speed, torque, and initial transient currents were calculated similarly to the standard 3-φ drives. The dual-inverter fed motors for traction systems as well as adjustable 3-φ drivers with open-end winding[7] for a variety of applications. Traditional multilevel converters have issues with voltage imbalance. By employing a higher phase number, these are eliminated, and the switching states are raised in proportion.

To analyses the probable causes of the proposed motor's defects in a 5-IM[8]. There are numerous methods for avoiding bearing problems, however costs can vary depending on the equipment configurations utilized to do so. The author contrasts the performance of the suggested motor with that of the existing motor and explains the key bearing flaws in his research. Different space vector approach patterns were used to drive the motor. DSP processing was used to analyze the results. The controllers are made to recognize the fault-tolerant drive system when the 3-φ IM is used in the D-Q axis model[9]. The researcher measured the motor's speed and torque and contrasted its proper operation with any malfunctions. To analyses the common mode voltage, the 5-φ IM drive is routed back to a 3-level neutral point clamped converter[10]. Typically, common mode voltage imbalances caused the existing drives to experience extreme swings. The proposed drive was examined both ways, taking into account common mode voltage effects. The modern control theory of new controllers which were developed to control the IM drive[11]. By using the controllers the proposed drive is suffered from few drawbacks. To overcome these drawbacks a precise controller was de-signed based on the modern control theory to enhance the performance of the proposed drive. A complete analysis of vector-controlled IM drive was operated with sensor less speed control with the unity p.f using fuzzy based speed full order observers[12]. Usual drawbacks were imbalances in the dc link, poor p.f, harmonics and input currents which are non sinusoidal, no power fed back to the source when conventional VSI operated with the IM drive. The suggested converter operates in a four-quadrant mode, eliminates undesirable harmonics, ensures sinusoidal input currents, regenerates power from source to load and vice versa, and responds quickly to system inputs, among other benefits. Two inverters were used in fixed rectifier and inverter modes to operate a new 4-level open phase IM drive[13]. Due to the dual mode of the inverters, a total of 64 voltage space vectors are built up here.

To enhance the performance of the suggested drive, zero state vectors were also to be excluded. 5-φ IM drive that was inverter- and LC filter-operated[14]. THD was examined after the harmonics were eliminated using filters. As an alternative to traditional methods of regulating using PWM, FOC, and DTC procedures, a DTC was presented[15]. Problems with typical inverters include pressure on motor bearings, high voltage stresses, common mode noise, and low power quality[16]. After a continues literature survey, it has been concluded in all the significant fields of the multiphase machine drives along with the conventional machine drives. All this precedent work has been initiated to analyze the research on multi phase drives. More accurately, the paper elaborated the advantages and drawbacks of proposed drives; hence it provides the scope of further opening of new pathway of research. Besides that the analysis considers an extensive research in terms of multi level inverter fed induction motor[17–24].

- *Increased efficiency* Multi-phase systems may be more energy-efficient and less expensive to operate because they may have lower conduction losses and less harmonic distortion.
- *Modular design* It is possible to construct multi-phase drives using a modular architecture, which makes maintenance easier, makes system expansion easier, and might even allow for continuous operation in the event that a module fails. This could result in more frequent system uptime, simpler repairs, and scalable systems that can expand to meet demand for power.

For PMSM drives fed by CHBMLI, traditional MPC might result in substantial switching losses, CMV and computational expense. It present a unique multiobjective FCS MPC that is based on VVB. This approach seeks to minimize switching losses between inverter modes, reduce the amount of calculations required (lowering computing cost), and lessen CMV.

To accomplish them, an offline optimization procedure is employed. This removes the requirement for detailed modifying while in use[25]. In[26] performance problems may arise from the traditional MPCC sensitivity to changes in the system's parameters. Because MFPCC does not reliant on a system model, it provides an alternative. It is therefore less susceptible to changes in the parameters.

To anticipate optimal control loop performance, however, MFPCC needs to continuously update its saved Current variations for every VSI state. These updates are necessary. The quantity of possible states in a VSI rises as the total number of voltage levels in the VSI grows. Considering it can only modify one current variation at a time throughout every sampling period, this presents a problem for MFPCC. The pace of update for individual current variations decreases with the number of states growing. The paper introduces two methods to deal with this problem: As a result, fewer viable options are taken into account for the subsequent control phase, increasing

the efficiency of the prediction process. By updating current variations intelligently, this approach makes up for the slower update rate of each current variation. In[27] this study investigates vector control and DTC, two potent control schemes for five-phase induction motors. In comparison to conventional three-phase control, both approaches achieve better performance by utilizing the advantages of a five-phase arrangement. The five-phase motor receives outstanding drive performance with vector control. The magnetic flux profile and current waveforms are shaped into a nearly rectangular shape as a result, which causes: like enhanced air gap flux density, which fortifies the magnetic field of the motor and a remarkable 10% increase in output torque over baseline control techniques. A major benefit of the five-phase inverter is that it has 32 space voltage vectors accessible, whereas a three-phase system only has 8. This abundance makes it possible to optimize the control algorithm and manipulate torque and magnetic flux precisely. When DTC is used in a five-phase motor, torque and magnetic flux variations (ripples) are substantially reduced, leading to exceptionally precise and smooth operation. This study makes a strong argument for the use of DTC and vector control in the regulation of five-phase induction motors. These cutting-edge methods provide notable performance gains by utilizing the five-phase configuration's fundamental benefits. In[28] precise current control is provided by traditional MPCC for multilevel converters (e.g., Cascaded H-bridge inverters).

It forecasts all potential voltage vectors' future current values and chooses the one that minimizes a cost function, which is frequently connected to monitoring a desired current reference[29,30].

However, a multilevel converter's huge number of accessible voltage vectors causes a significant increase in the amount of calculations required for prediction. Due of this computational load, typical control platforms with little processing capacity may find it difficult to implement MPCC. In this study, a modified MPCC technique that requires a much fewer amount of calculations is introduced. This change is made without affecting the system's accuracy of present control performance. The paper conducts trials with both five-level and nine-level inverters to validate the efficacy of the suggested approach.

This study tackles the high computational cost of MPCC, which is a major drawback for multilevel converters. The revised approach that has been suggested provides a workable answer by cutting down on computations without compromising control performance. This makes it possible to apply the advantages of MPCC—precise current control—in a wider range of multilevel converter applications by paving the way for its implementation on common control platforms.

A detailed examination of the literature review of Optimizing Electric Vehicle Charging Stations has presented Table 1.

This reference provides an example of a three-phase cascaded H-Bridge inverter multi-objective MPC approach for a PMSM. Application and analysis of this method for five-phase induction motors are lacking[25]. The MPC for a three-phase cascaded H-Bridge inverter is demonstrated in this reference. Application and analysis of MPC for five-phase inverters are lacking[28]. While DTC and vector control are highlighted in this reference, other sophisticated control techniques, such as Model Predictive Control (MPC) for five-phase motors, are not as well explored[27].

Based on the above research gaps, the novelty of this research is as follows:

Multiple-objective MPC has been shown in the literature to be capable of improving many elements of electric motor drives. Some implementations are computationally complex, for example, which is one of their constraints. By concentrating on IPDPWM control used on an FPGA controller for a five-phase induction motor drive, this proposed work offers a unique methodology. This method completely avoids the use of MPC. The following is how work fills the research gap:

- *Alternative control strategy* Investigate IPD PWM, a less complex carrier-based PWM technique, as an alternative to MPC that may reduce computing complexity. For real-time control applications wherein reducing processing delays is essential, this might be especially helpful.

Reference	Focus	Methodology	Key findings	Research implications
[25]	CHB-MLI-based multi-objective MPC for PMSM drives	MPC is voltage vector-based finite control set (VVB-FCS)	Reduces CMV switching losses, and computational costs. Attained by use of offline optimization	New VVB-FCS MPC provides effective control with lower CMV and complication. creates opportunities for additional study on power sharing optimization, switching frequency, and CMV dv/dt mitigation
[26]	Expansion of multilevel VSI MFPCC	Extended adjacent state scheme for MFPCC—resolves model-based PCC's parameter sensitivity concern	Retains acceptable performance in multilevel VSIs with less computational strain	For multilevel VSIs, MFPCC with enhanced adjacent state scheme provides reliable current control. Emphasizes MFPCC's potential for a range of multi-layer inverter applications
[27]	Five-phase induction motor control	Vector control and direct torque control: this method achieves increased torque and the required current waveforms with high control precision	Both techniques work well with 32-bit DSPs on five-phase motors	Strengthens existing control procedures for multi-phase motor control (vector control, DTC) that have been proven effective
[28]	Multilevel inverter MPC	Modified CHB inverter MPC	A lighter computational load on MPC systems	Multilevel inverters' efficacy was verified. allows for the previously complicated application of MPC to a variety of multi-level inverter topologies

Table 1. Research studies for multi-phase induction motor drives.

- *FPGA implementation* There may be advantages to using an FPGA controller when putting IPD PWM into practice. Relative to conventional DSPs, FPGAs provide hardware-level parallelism, that can be useful for real-time control tasks. This might speed up the control algorithm's execution and enhance system performance as a whole.

In the preceding section III, a concise operation of 2-level five leg (5-leg) inverter is discussed. In section III, the advantages of multi level inverters along with the proposed CHBMLI inverter are presented. In section IV, the modeling and fabrication 5-φ IM are discussed. To know the dynamic performance of the proposed drive under various frequencies, *V/f* technique is used. Finally, in section VI, the proposed CHBMLI fed five phase IM drive experimental verification is illustrated. The laboratory experimental setup shows the analysed results and it carries the beneficial conclusions of this proposed work.

2-Level five phase VSI

1-φ and 3-φ inverters are generally considered for low and medium power applications. For high power applications multilevel inverters are introduced with number of phases (legs) are increased. Here 5-φ topology is developed to control amplitude and frequency and thus reduce the harmonic content with increased efficiency. In this paper before going to discuss the multi level inverters, 2-level 5-Leg voltage source inverter operation has to be illustrated[17]. The 5-Leg VSI topology is represented in Fig. 1 with 10 switches having a phase delay of 36°, where each phase conducts about 72° with the help of top and bottom leg switches respectively S_1, S_3, S_5, S_7, S_9 and S_6, S_8, S_{10}, S_2, S_4. The proposed two level VSI operated in 10 intervals. For every interval 5 switches are conducted among them, 2-switches are from top group and 3-switches from the bottom group or vice versa. Every leg is operated for 72° only. The switching devices are turned ON and OFF at their regular sequence given intervals respectively with effective conduction and to avoid the short circuit. For interval I, 0°ωt 36°, S_1, S_8, S_{10}, S_7, S_9 are in conduction mode. All the corresponding intervals are tabulated in Table 2. Furthermore, the other switches are in conduction mode basing on their operating sequence. In this operating mode, here three impedances are connected in parallel with positive polarity and two impedances are connected with negative polarity to meet the required output[18–23].

Operating modes are explained in detail, for half period of cycle. Here 5 switches are operated for every conduction mode. Conduction of switches for upper leg is shown in red color and lower leg switches is shown in green color. In this mode I, during $0^0 \leq \omega t \leq 30^0$ upper leg switches 1, 7, 9 are turned on and 8, 10 are from the lower leg switches are turned on shown in Fig. 2. The equivalent circuit current, phase and line voltages are Calculated and shown in (1), (2) and (3). Line voltages are determined from the calculated phase voltages. The switches are used for experimental set up in Fig. 3.

From the equivalent circuit current calculated, as shown in (1)

$$i_1 = \frac{v_s}{\frac{5z}{6}} = \frac{\frac{6}{5} * v_s}{z} \tag{1}$$

Phase voltages are calculated, as shown in (2) and (3)

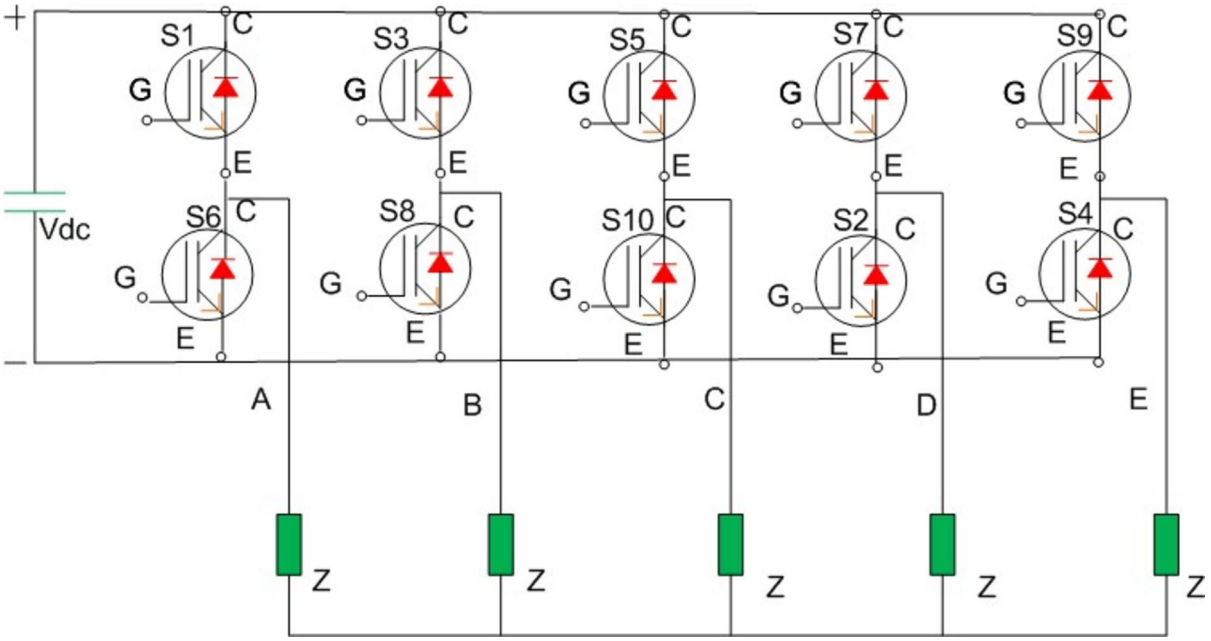

Figure 1. Proposed 2-level 5-leg inverter.

Intervals	Duration of intervals	Conduction switches
I	$0 \leq \omega t \leq 36°$	$S_1S_7S_8S_9S_{10}$
II	$36° \leq \omega t \leq\leq 72°$	$S_1S_2S_8S_9S_{10}$
III	$72° \leq \omega t \leq\leq 108°$	$S_1S_2S_3S_9S_{10}$
IV	$108° \leq \omega t \leq\leq 144°$	$S_1S_2S_3S_4S_{10}$
V	$144° \leq \omega t \leq\leq 180°$	$S_1S_2S_3S_4S_5$
VI	$180 \leq \omega t \leq\leq 216°$	$S_2S_3S_4S_5S_6$
VII	$216° \leq \omega t \leq\leq 252°$	$S_3S_4S_5S_6S_7$
VIII	$252 \leq \omega t \leq\leq 288°$	$S_4S_5S_6S_7S_8$
IX	$288° \leq \omega t \leq\leq 324°$	$S_5S_6S_7S_8S_9$
X	$324° \leq \omega t \leq\leq 360°$	$S_6S_7S_8S_9S_{10}$

Table 2. Operating intervals of proposed 2-level inverter.

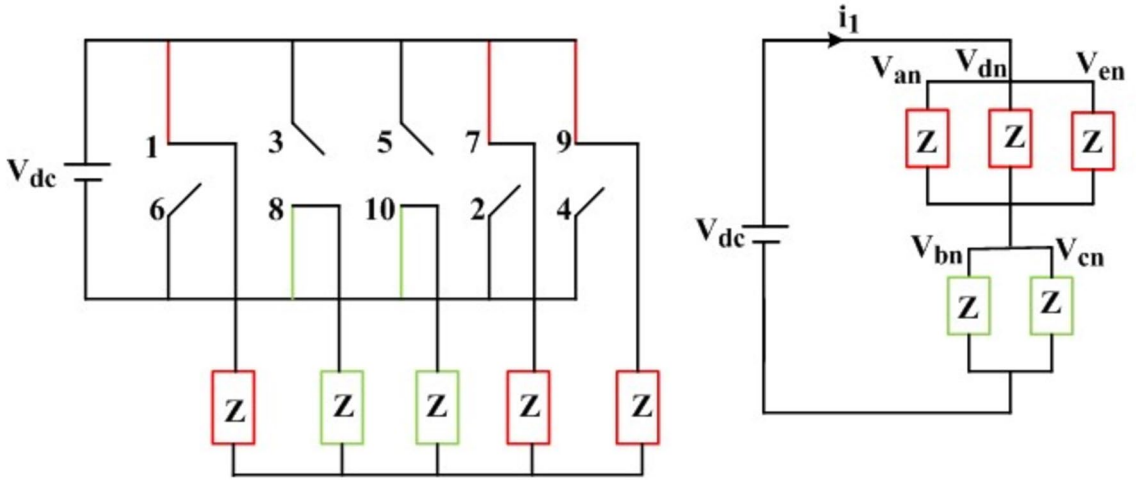

Figure 2. Proposed 2-level 5-leg inverter equivalent circuit in MODE-I.

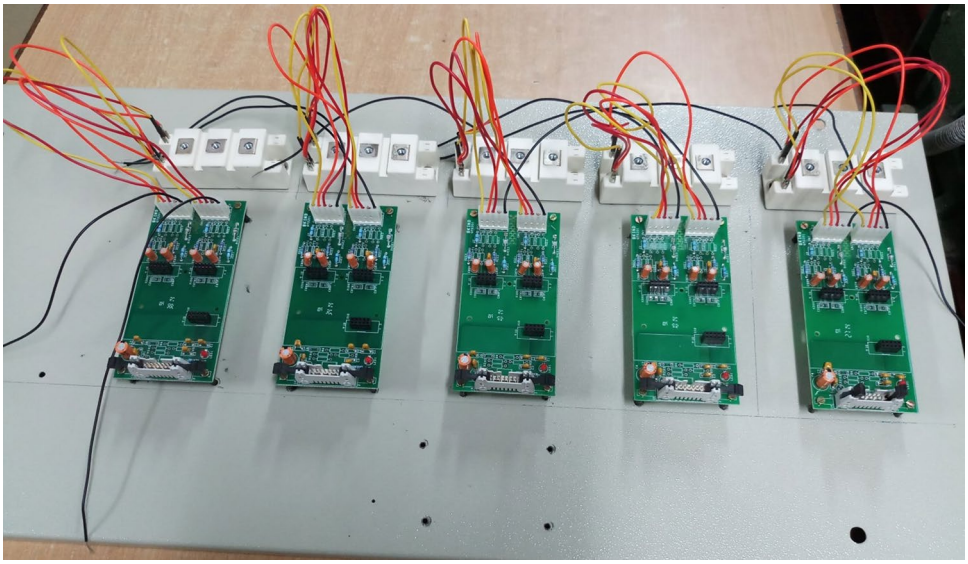

Figure 3. Proposed 2-level 5-leg inverter switches.

$$V_{an} = V_{dn} = V_{en} = \frac{i_1 * z}{3} = \frac{2}{5} V_s \tag{2}$$

$$V_{bn} = V_{en} = \frac{-i_1 * Z}{2} = \frac{-3}{5} V_s \tag{3}$$

It provides the pulses for all the 5-legs of the inverter switches. Here, carrier frequency should be considered in terms of the reference wave as 5th multiples and therefore the 5th order harmonics are eliminated. For the 5-leg inverter one carrier wave and five reference signals are used to develop the gating signals as shown in Fig. 4. Hence total harmonic distortion and noise levels are reduced during the operation of the inverter. Thus it further increases the performance of the inverter. In order to drive the FPIM with 5-leg inverter this gives the efficient operation of the drive. To get variable voltage and variable frequency one need go for PWM schemes. SPWM is one of the PWM technique applied to inverters of 2-Leg, 3-Leg and 5-Leg to achieve variable voltage and variable frequency by varying Modulation Index and f_r respectively. Space vector modulation technique due to digital implementation makes the control complex. Analyze the speed of Induction Motor without affecting air gap flux by varying the voltage and frequency. So when Voltage varied frequency also vary proportionally to maintain air gap flux constant such that power factor, as well as maximum torque capability of the machine remains unchanged.

Proposed five phase cascaded H bridge inverter

Inverters are plays a essential role in the present field of power management, particularly in the rural areas almost two billion people are not to access the power supply for their utilities. Therefore various multilevel inverter topologies are introduced from conventional to advanced configurations are developed. In this work, mainly focuses on five phase 2, 3 and 5 level cascaded H-bridge multi level inverters total harmonic distortions are elaborated. for applications requiring strict power quality, the five-level CHBMLI offers a novel method for producing high-quality output waveforms. To achieve five levels, typical multi-level inverters could need three different structures; in contrast, the CHBMLI uses a single, compact design to do this. This may result in a decrease in the overall cost of the system in addition to reducing complexity. The ability of the five-level CHBMLI to provide an output voltage waveform that is almost sinusoidal is its main advantage. In order to accomplish this, five different voltage levels are produced at the output (S1, S2, S3, S4): +Vdc, 0, −Vdc, +2Vdc, and −2Vdc. The manner in which particular switching combinations of these four switches produce the required voltage levels is described in Table 3 for switching states and voltage levels. This is a condensed explanation:

- Levels of +Vdc and −Vdc:
  Switch combinations (S1 & S4 or S2 & S3) that are activated cause the output to achieve +Vdc or −Vdc, respectively.
- Absolute voltage:
  The output voltage drops to zero when both switch pairs (S1 & S4 and S2 & S3) are off.
- Optional +2Vdc and −2Vdc levels:
  By combining both DC sources in series with particular switch combinations, these higher voltage levels can be reached. It's crucial to remember that these particular levels require equal DC voltage sources. Compared to conventional two-level inverters, the capacity to produce these five voltage levels greatly decreases harmonic distortion in the output waveform, improving power quality. Compared to conventional two-level inverters, the capacity to produce these five voltage levels greatly decreases harmonic distortion in the output waveform, improving power quality.

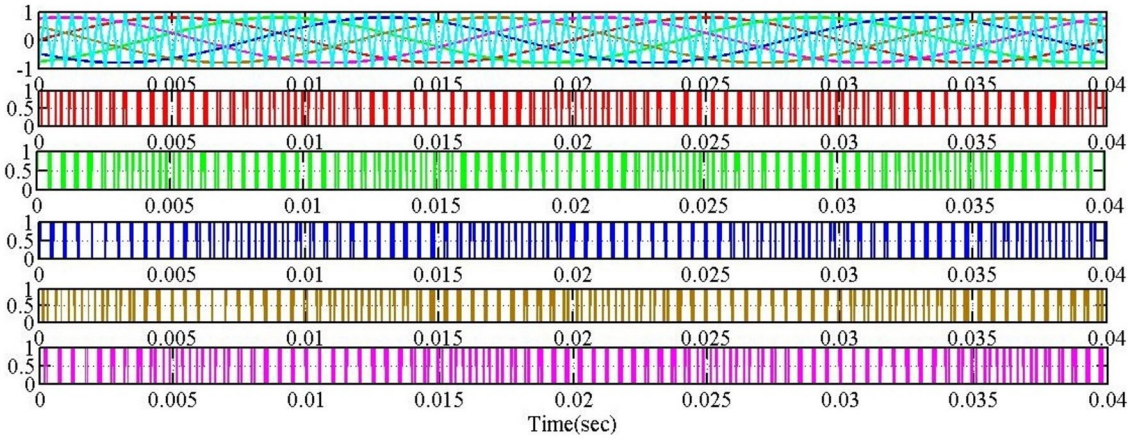

Figure 4. Proposed 2-level 5-leg inverter gating pulse generation using SPWM technique.

S_1	S_3	S_1'	S_3'	V_{out}
ON	OFF	ON	OFF	2 V_{dc}
ON	ON	ON	OFF	V_{dc}
ON	OFF	ON	ON	V_{dc}
OFF	OFF	ON	OFF	V_{dc}
ON	OFF	OFF	OFF	V_{dc}
ON	ON	ON	ON	0
ON	ON	OFF	OFF	0
ON	OFF	OFF	ON	0
OFF	ON	ON	OFF	0
OFF	OFF	ON	ON	0
OFF	OFF	OFF	OFF	0
ON	ON	OFF	ON	$-V_{dc}$
OFF	OFF	OFF	ON	$-V_{dc}$
OFF	ON	OFF	OFF	$-V_{dc}$
OFF	ON	ON	ON	$-V_{dc}$
OFF	ON	OFF	ON	$-2V_{dc}$

Table 3. Switching table for proposed CHBMLI.

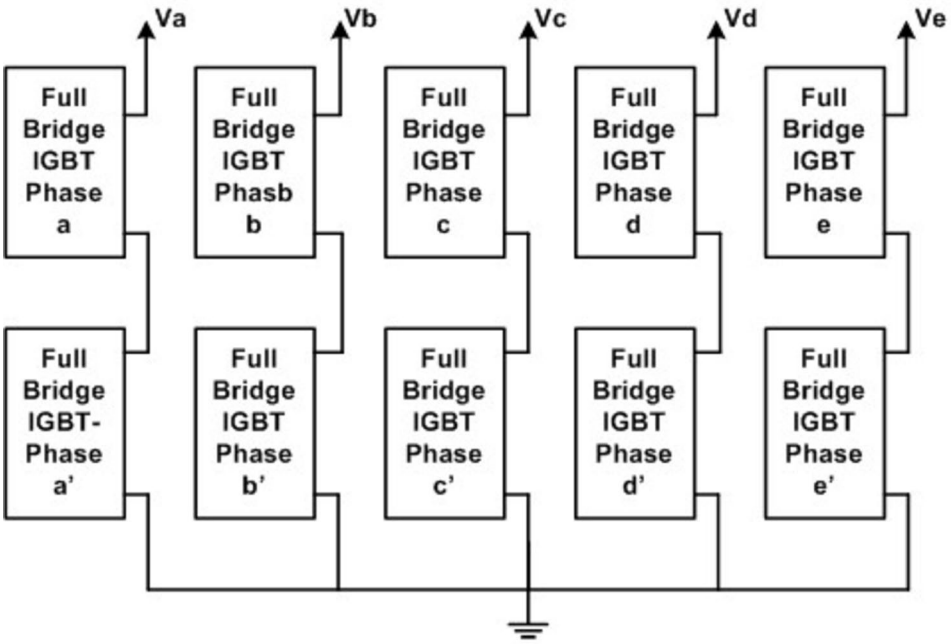

Figure 5. Schematic diagram of proposed CHBML inverter.

The proposed CHBML inverter schematic circuit is shown in Fig. 5 and single leg circuit shown in Fig. 6. Two steps are necessary to implement the hardware module of proposed multilevel inverter. The first step to develop the control circuit and then power circuit are implanted. The driver circuit and isolation circuits are placed in the control circuit, it is also used to develop the gating pulses by using the specified PWM techniques, whereas the second circuit consists of supply and power processing systems.

A particular kind of level-shifted PWM called IPD PWM occurs when all carrier signals have the same frequency and phase alignment. Every carrier signal is independently compared to the reference signal. A high voltage level is produced as the output when the reference signal exceeds the carrier signal. A low voltage level is produced as the output when the reference signal is less than the carrier signal. Corresponding signals are produced, as depicted in Fig. 7 generating gating pulses logic in the flowchart format depicted in Fig. 8 for the proposed CHBLMI.

Compared to conventional two-level inverters, multi-level inverters have a number of benefits. The lower common-mode voltage is a major advantage since it can ease the strain on the motor and possibly lengthen its life. Multi-level inverters can also draw input current with less distortion, which improves the overall quality of the power. A greater range of switching frequencies can be used by these inverters to function. Higher efficiency

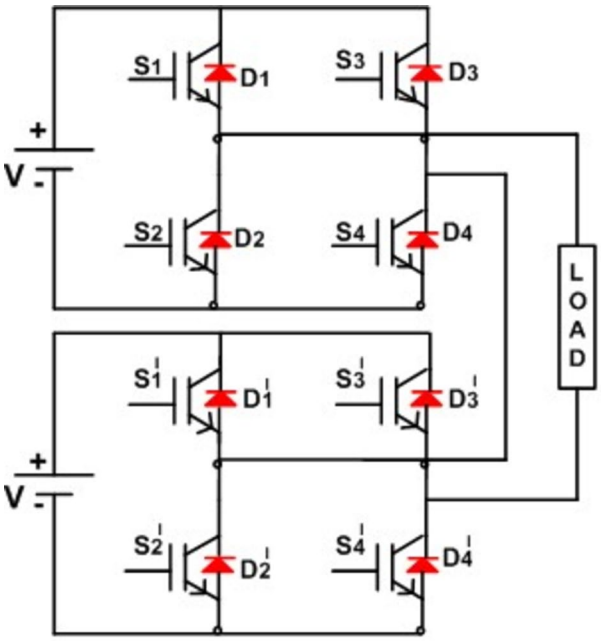

Figure 6. Single leg power circuit configuration of proposed CHBML inverter.

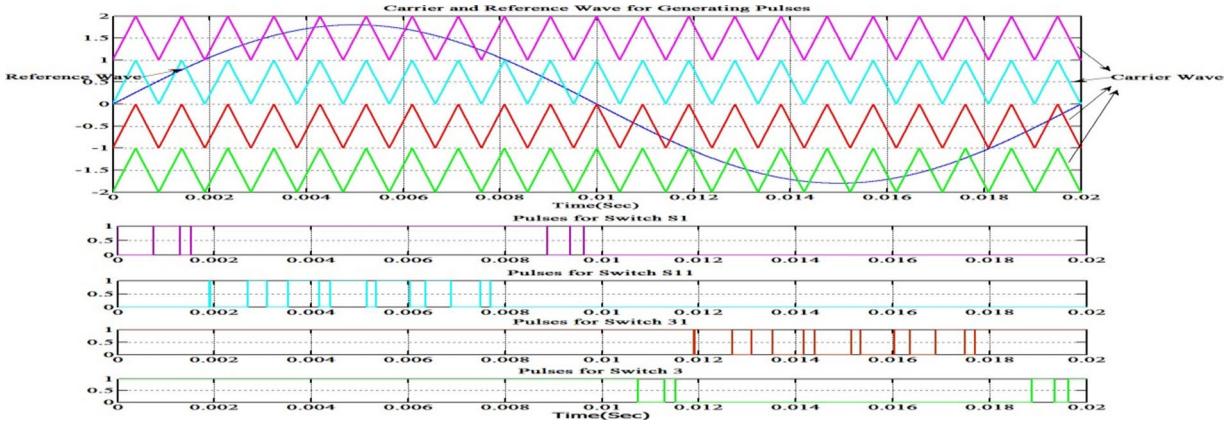

Figure 7. Carrier wave and reference wave to generate the gating pulses to the proposed CHBML inverter.

and reduced switching losses are directly correlated with lower switching frequencies. However, the output waveform may experience potentially more harmonic distortion as a result of this. A greater switching frequency may be required in order to obtain low THD without the need of further filtering.

Comparing the suggested five-level inverter topology to traditional cascaded H-bridge multi-level inverters, it provides a novel method with fewer active devices. This design produces five different output voltage levels using the PD technique. It accomplishes this using fewer components, which lowers system complexity and might cut costs. The capacity of this suggested topology to function at lower switching frequencies is one of its main advantages. Efficiency is increased because switching losses are reduced at these lower frequencies. In order to ensure correct inverter functioning, it is assumed that the explanation of the switching process for the upper leg switches has a corresponding operation for the lower leg switches.

The designed CHBML inverter output fed to 5-φ squirrel cage induction motor drive. A well known open loop V/f technique is used to know the dynamic performance of a proposed drive and it is implemented on XilinkSparton6 FPGA processor. The Xilink Sparton6 FPGA controller and the driver circuit is shown in Figs. 9 and 10. The entire proposed Hardware setup along with the internal architecture that is 5-φ 5-level CHBML inverter as shown in Fig. 11.

A flexible semiconductor that may be configured to carry out a variety of digital functions is the Xilinx Spartan-6 FPGA. Because of this, it's a good platform for managing multi-level inverters. As opposed to conventional two-level inverters, these inverters produce output waveforms that are more complicated. A plethora of tools is provided by the Spartan-6 to accomplish this control. The configurable logic block is the CLB. Consider these CLBs as small modular components that can be configured to carry out particular logic functions. These CLBs

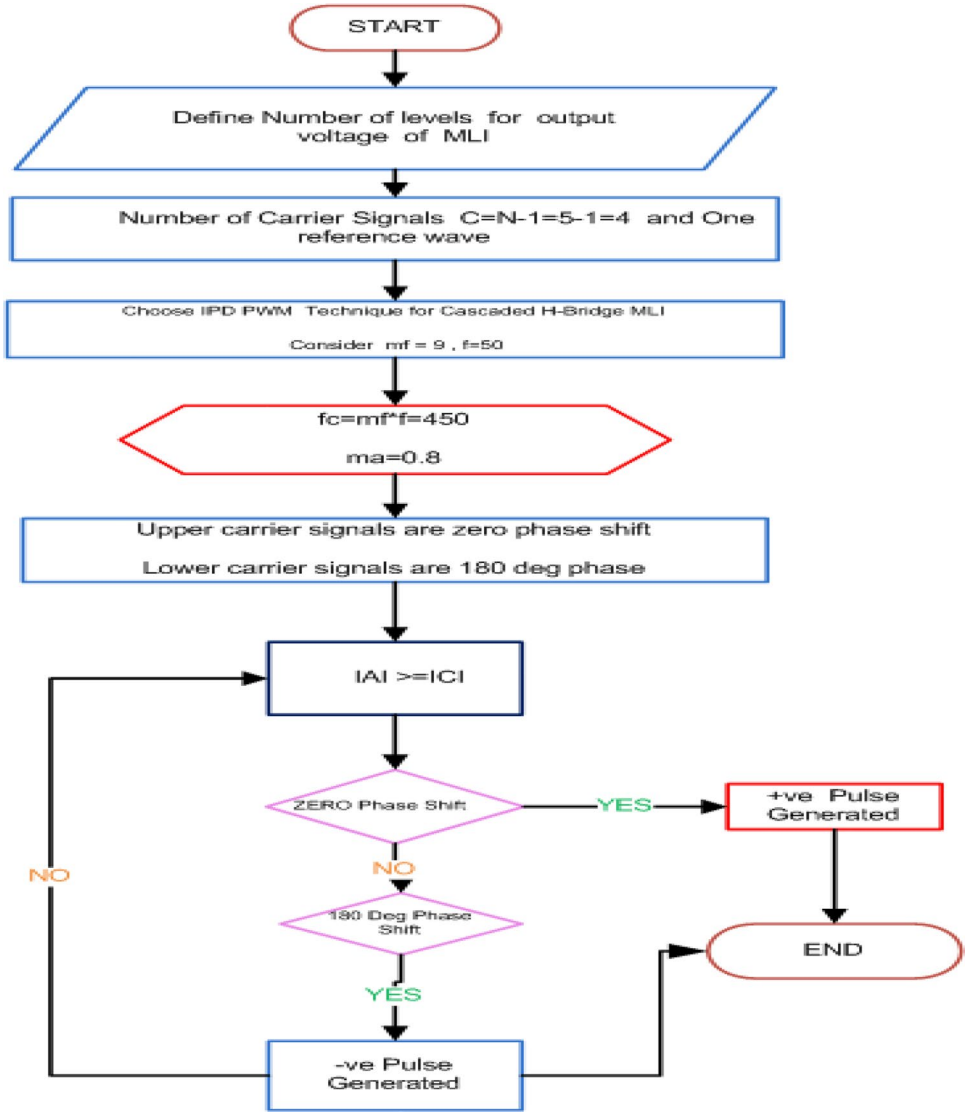

Figure 8. Flow chart for CHBLMI using IPDPWM technique.

have been programmed to implement the control algorithms required by multi-level inverters in order to produce the proper waveform output. The Spartan-6 occasionally offers DSP slices as well. These are specific regions on the chip that are capable of effectively handling calculations that are more sophisticated. These DSP slices can be a useful tool for multi-level inverters with especially complex control algorithms. All things considered, the versatility and resource range of the Spartan-6 FPGA make it an effective instrument for managing and implementing complex functionality in multi-level inverter systems.

- Steps to implement a multilevel inverter on Spartan-6 FPGA:

  - *System design and specification* This preliminary stage establishes the parameters of the inverter, such as the quantity of output voltage levels, the modulation method of choice for managing the output waveform, and control schemes for accomplishing the intended behavior.
  - *HDL coding* The functionality of the inverter is described in Verilog or VHDL. Determining modules, signals, and the ways in which different FPGA components interact are all part of this process.
  - *Technique of modulation application* The HDL code applies the selected modulation method, such as SPWM. This establishes how the inverter's switching signals are created from the reference signal.
  - *Control logic development* This involves converting the intended output waveform into distinct switching states for the switches in the inverter. These switching states can be computed dynamically or by referencing them from a pre-defined Table 2.
  - *PWM signal generation* Depending on the selected modulation strategy, the FPGA's internal resources, like as comparators and counters, are used to produce exact PWM signals.

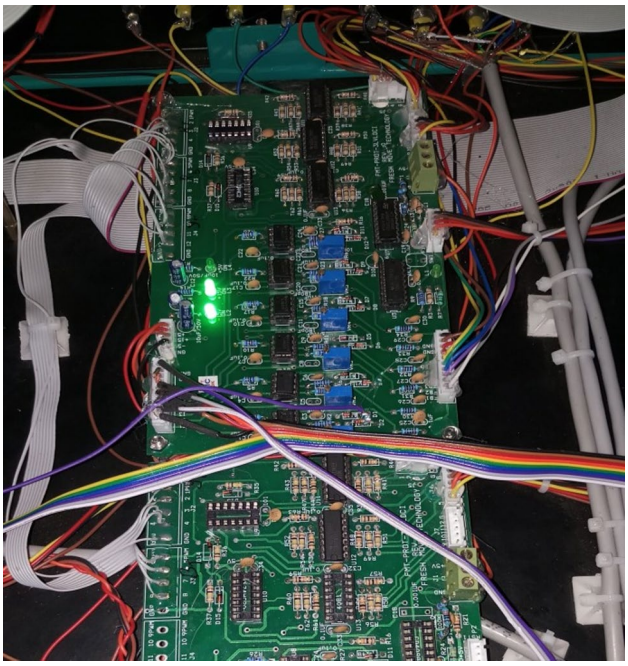

Figure 9. XC6SLX9FPGA controller.

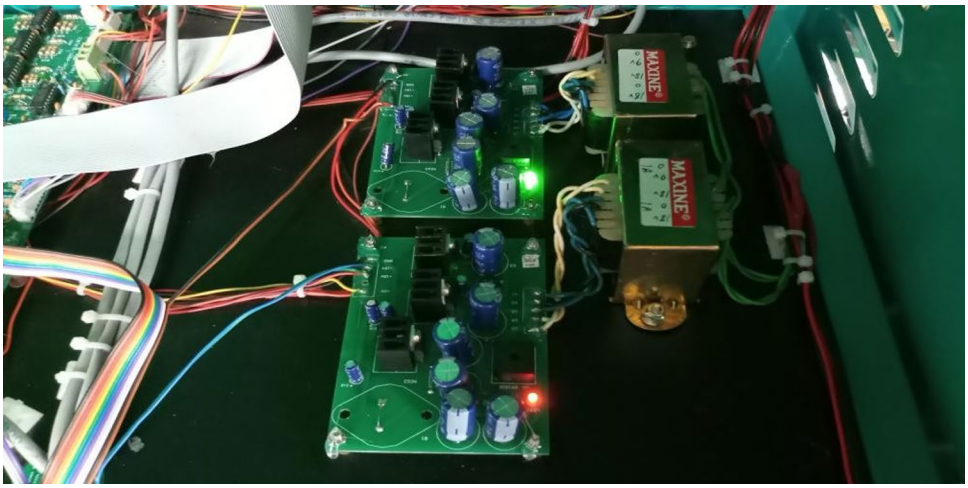

Figure 10. Driver circuit for the CHBML inverter.

- *DSP* The Spartan-6's DSP slices may be utilized for intricate control algorithms or signal processing activities.
- *Interface design* The FPGA is connected to external power electronics components, such as gate drivers for the inverter switches, through interfaces.
- *Simulation and verification* It is essential to use FPGA simulation tools to simulate the design before implementing it on hardware. This guarantees that the inverter will function as intended and fulfill its design specifications.
- *Synthesis and implementation* The HDL code is converted into a format that the Spartan-6 FPGA can understand using the Xilinx ISE or Vivado tools. Logic synthesis and adapting the design to the FPGA's capabilities are involved in this procedure.
- *Hardware testing* Lastly, the design is put to the test on a hardware platform using the real power electronics components. This enables for any necessary tweaks and confirms that the entire system works in a real-world setting.

While using a Spartan-6 FPGA to create a multilevel inverter provides flexibility for intricate control algorithms, there are some important factors to keep in mind for an effective implementation:

Figure 11. 5kVA 5 level configuration of proposed CHBMLI.

- *Resource utilization* Resources such as CLB's and DSP slices are limited on the Spartan-6. By making the most efficient use of these resources possible through HDL code optimization, more features or more complex control logic may be possible while still maintaining the capacity.
- *Clock management* Multilevel inverters require precise and coordinated control. The clock management capabilities of the Spartan-6 can be employed to produce and disperse clock signals across the architecture, guaranteeing accurate timing and synchronization of diverse elements.
- *I/O configuration* In order to communicate with external power electronics components, the FPGA's I/O pins must be set up correctly. To ensure appropriate communication, pin directions (input/output) and voltage levels must be defined.
- *Power supply* The Spartan-6 FPGA and the linked power circuits must both operate reliably, hence maintaining a steady and sufficient power supply is essential. It's crucial to adhere to the suggested power supply standards and have good power integrity procedures in place.
- It is possible to create multilayer inverters with complex control algorithms on the Spartan-6 FPGA by taking these aspects into account and using effective coding techniques. Thorough testing at every stage of the development process guarantees that the design satisfies performance objectives and operates dependably in an actual setting.

A flexible framework for integrating control algorithms and signal processing in multi-level inverters, including five-phase designs, is provided by the Xilinx Spartan-6 FPGA. To achieve this capability, a number of essential elements are required:

- *CLBs* Modulating and controlling the inverter requires the implementation of digital logic, which is provided by CLB's, the building blocks of the architecture.
- *DSP slices* These specialized resources offer sophisticated algorithms hardware acceleration. DSP slices can be applied to specialized modulation techniques, signal processing jobs, or sophisticated control strategies in a multi-level inverter.
- *Block RAM* Information, settings, and intermediate outcomes required for inverter operation are stored in this on-chip memory. When buffering and controlling real-time data streams, it's especially helpful.
- *IOBs, or input/output blocks*, are responsible for controlling communication between the FPGA and external parts. Interfaces between sensors, gate drivers for the inverter switches, and communication modules are handled by IOBs in multi-level inverters.
- *The clock distribution resources and DCM's* For an inverter to operate accurately, timing must be precise. Clock distribution resources make sure that clock signals are distributed synchronously to all areas of the design, whereas DCMs create and maintain the clock signals.

- *HCB's* These provide for an organized design process, which in turn allows for effective communication and organization inside the FPGA. Managing intricate multi-level inverter control logic can benefit from this.
- *Fault detection and protection logic* This logic, which is implemented with the help of CLBs, keeps an eye out for irregularities in the inverter's functioning and sets off preventative measures to avoid damage.
- *Select IO technology* Differential signaling is one of the input/output standards that IOBs can be set to handle. For reliable connectivity with external sensors and components, this is crucial.
- *Configuration memory and power management circuitry* Power management circuitry optimizes power consumption in accordance with operational requirements, while configuration memory holds the bitstream that describes how the FPGA operates.* The Spartan-6 FPGA can be used to develop control algorithms, modulation strategies, and interfaces that are specifically designed to meet the needs of the multi-level inverter application by properly setting these components. The Spartan-6 is an effective platform for implementing intricate and adaptive control techniques in multi-phase inverters because of its programmability and versatility

The proposed SPWM control algorithm developed by using front end mode with the sampling frequency is10kHz. This developed code fed to XilinkSparton 6 FPGA processor, then respective gating pulses are produced. The over loading conditions and short conditions are occurred in the circuit, then the power circuit components are protected by using current sensors and continues monitoring on load currents for the power module with a small ON/OFF switch.

In the proposed module there are 40 IGBT switches are used with the rating of 1200 V, 100A, Each H-bridge consist of four switches with anti parallel diodes utterly 10 H-bridges are used to form 5-φ 5-level with the proper heat sink. Snubber capacitor provided for each H-bridge for dv/dt protection. 40 HCPL316J IC based driver circuits are used to isolate and drive IGBT PWM signals. Isolated Regulated power supply rating @ + 15 V/0.5A Used for IGBT PWM driver circuits. Ten current sensors are used to sense the all sensor outputs are used for current protection and over load Trips, terminated in front panel for measurement purpose. Also five CT's are used to sense the five phase load currents. Necessary Interfacing connectors provided for PWM Input from FPGA controller and analog outputs to FPGA controller. All PWM signals terminated in front panel through BS2 connector. The PWM pulses are become able to be seen using CRO. Overload trip and indication circuit is available along with the overload fuse protection. These are all components are enclosed with a nice industrial type of cabinet and front panel.

For multi-level inverters to operate safely and dependably, strong protective systems are needed. This calls for the integration of sensors, complex control algorithms, and communication protocols. Regular testing and calibration are also essential to keep these mechanisms operating at peak efficiency.

The following are important things to keep in mind when safeguarding a multi-level inverter system, which includes the FPGA controller:

- *Protection and monitoring of current* Power electronics components' current flow is continuously observed by sensors. The control system takes corrective action, which may involve deactivating a problematic phase or shutting down the inverter altogether, if a current exceed a safe limit.
- *Voltage monitoring and protection* Voltage levels are monitored by voltage sensors at crucial locations such as the DC bus and output terminals. In order to prevent damage, the control system may cut output power or shut down if voltages exceed or fall below acceptable operating ranges.
- *Temperature management* The control system receives data from temperature sensors on vital parts such as inductors and power semiconductors. In order to prevent thermal damage, the system can cut power output, turn on cooling devices, or shut down if temperatures climb above safe thresholds.
- *Protection against short circuits* Circuit breakers and current sensors cooperate to identify and separate short circuits. In the event of a short circuit, the control system can promptly identify the issue and stop additional harm.
- *Communication-based protection* Feedback from sensors and other components is received by the control system via communication protocols. The system has the ability to take preventative action, such as shutting down or isolating the impacted area, if communication disturbances are found.
- *Fault diagnostics and logging* System parameters can be continually monitored and recorded by the control system. Post-fault analysis can be performed on this data to find the underlying causes of failures and carry out future corrective measures. Multi-level inverter systems, like the CHBLMI, may operate safely and dependably by putting these thorough protective mechanisms into practice.

Proposed five phase induction motor drive

Usually, 90% of the ac motors are IM's, which are used in the industrial and large power applications. There is endless research is going on ac machine drives. Due to few drawbacks in the conventional 3-φ motors, a high phase number of motors can be introduced since it has inherent advantages. There are numerous key points of the proposed IM than conventional 3-φ machines.

i. A rotating field with fewer harmonics is created whenever the stator is excited from the supply while the machine is operating at a higher phase number.
ii. In traditional motors, if a phase is opened while the motor is running, it continues to operate solely with the additional equipment; however, in the proposed motor, it continues to operate without any further equipment.

iii. Compared to conventional motors, multiphase machines exhibit less torque ripple.

Stationary five voltage axes are renewed into two phases as shown in Fig. 12. For fabrication of 5-φ IM, consider a 3-φ IM and remove the total winding and rearrange the windings as per the requirement. The slots are multiples of five for the proposed drivebutintraditional3-φIMslotsarearrangedinmultiples of three only.

The five-phase permanent magnet motor (FPIM) discussed in this section is made to run even in situations where there is a little discrepancy between the number of stator slots and the required number of phases. This motor exhibits successful performance with a slight deviation, whereas a conventional five-phase motor can have an even number of slots divisible by five as shown in Figs. 13 and 14. The idea does, however, demonstrate the motor's capability to operate well in spite of the slight slot shortfall. To attain the necessary five-phase supply, the winding connections deliberately make use of particular slots. In cases where a perfect number of slots would not be possible because to limits or design constraints, this strategy may be advantageous. For a more thorough understanding, greater research into the particular winding connections and how they affect performance would be beneficial.

For fabrication of 5-Φ IM, consider a 3-Φ IM and remove the total winding and rearrange the windings as per the requirement. The slots are multiples of five for the proposed drive but in traditional 3-Φ IM slots are arranged in multiples of three only.

Figure 15 shows the squirrel cage rotor and 24 slots,4 -pole stator of 3-Φ IM. By using conventional motor the FPIM is fabricated. Here 5-Φ stator core slots are multiples of five, hence to fabricate for desired output, 2-pole machine was fabricated instead of 4-poles. Slots are reduced to 20 for the proposed motor. Four slots are left with

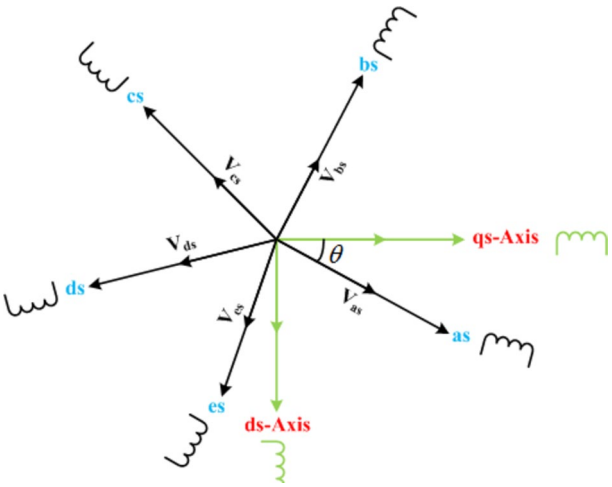

Figure 12. Modelling of FPIM 5-φ to 2-φ conversion.

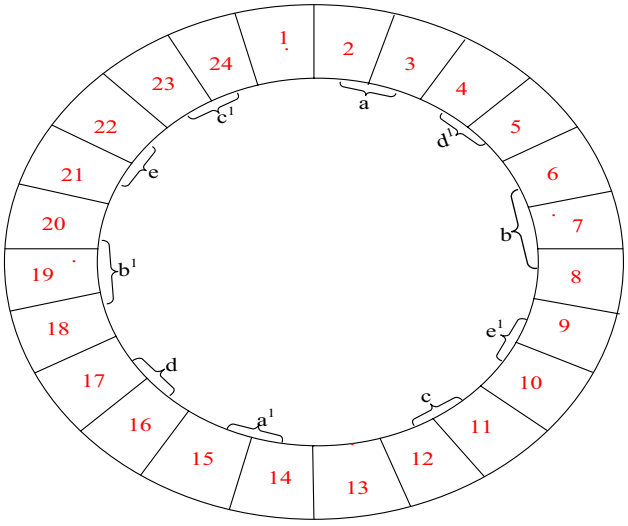

Figure 13. Winding slots of FPIM.

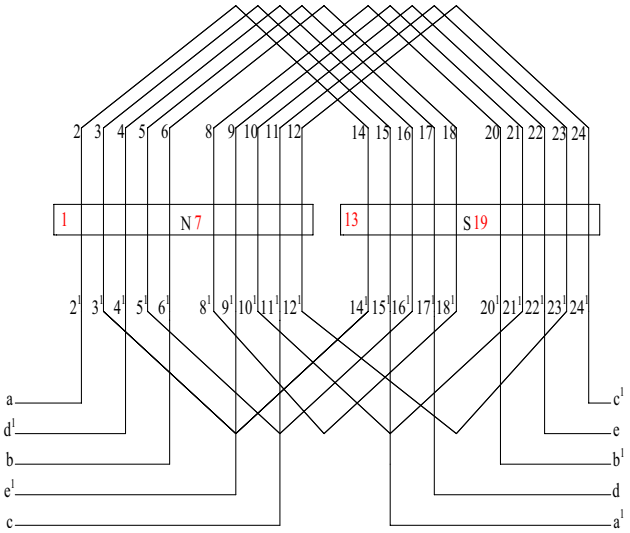

Figure 14. Winding diagram of FPIM.

Figure 15. (**a**) Conventional 3 phase IM stator and rotor. (**b**) Proposed FPIM stator core.

no winding. Squirrel cage rotor is used instead of slip ring rotor because of rugged construction. Almost 90% of the motors equipped with cage rotor only which are all used for all industrial applications.

Final stator winding fabricated, and slots are filled with core as shown in Fig. 15, hence the respective output phases a, b, c, d, e along with the neutral point connection terminals such as a′, b′, c′, d′, e′[17,18,26–28].

For the testing and validate the results are obtained from the experimentation of the proposed scheme, a 1 kW squirrel cage FPIMD is fed from the CHBML Inverter with a constant V/f ratio mode in open loop and closed loop. Testing of the multilevel inverter unit with MECO 5850 power quality analyzer is used to know the order of harmonic content and performance parameters of Fig. 16. 5-φ 5-Level Phase voltages of Proposed CHBML Inverter proposed inverter at various load cases and frequencies. It gives the linear load variations at the inverter end.

Results and discussions

The power quality analyzer configuration used for testing the developed system is as shown in Fig. 12 and it shows the waveform for phase voltages at the output frequency of 50 Hz and 300 V, the waveform is obtained by using the Digital Storage Oscilloscope (DSO) with appropriate attenuation probes in turn to check the output voltages levels besides the power quality issues using power quality analyzer. The phasevoltages are captured for 50 Hz and are shown in Fig. 17. As the levels on the inverter side increases, it can reduce the dv/dt stress on the semiconductor switches and hence the Electro Magnetic Interferences (EMI) with the neighbouring systems.

The waveform exhibits the five levels on output voltage using the integrated experimental setup, similarly the triggering pulses from the FPGA for the power switches are captured using the DSO is shown in Fig. 13. Here,

Figure 16. Phase difference among the 5-φ voltage at 50 Hz.

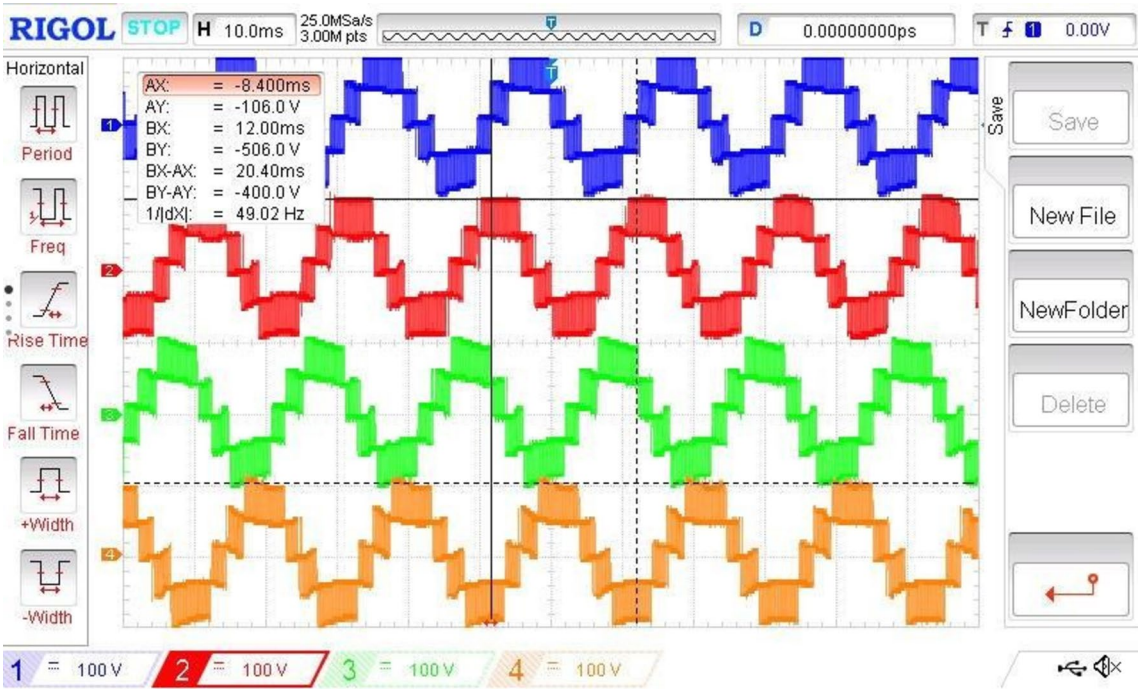

Figure 17. 5-φ 5-level phase voltages of proposed CHBML inverter.

the DSO consist only 4-Channel, hence the phase voltages V_a, V_b, V_c, V_d are visible out of the five phase voltages with an amplitude of 200 V and with a time delay of 72° w.r.t the reference. Figure 18 shows the line voltages (V_{ac}) of the proposed inverter with peak voltage of 484 V and takes a delay of 144° w.r.t the reference. By observing the Fig. 17 the no. of levels are increased, it is an level line voltage compared to the phase voltage of the proposed inverter there only it shows the five level output voltage.

Figure 19 shows the line voltages (V_{ab}) of the proposed inverter with peak voltage of 360 V and phase delay of 72° w.r.t the reference. By observing the Fig. 14 the no. of levels are increased, it is a seven level output line voltage compared to the phase voltage of the proposed inverter there only it shows the five level output voltage.

Figures 20 and 21 shows the gating pulses for one single phase of the proposed inverter out of five phase.

Here each phase consists of eight switches that means four switches for upper leg and other four switches for lower leg to form a proposed CHBML Inverter. Here the pulses are generated by using the SPWM technique. The proposed CHBML inverter fed to resistive load before fed to the FPIM.

Figure 22 shows the phase currents with a magnitude of 2A. The current waveform follows the phase voltage waveform because the voltage and current are in phase with the resistive load. The proposed CHBML inverter fed to the FPIM. Figure 23 shows the phase currents with a magnitude of 1.8A. Here, the motor load acts as a RL load, the current waveform is approximately sinusoidal.

From Table 4 the proposed CHBML inverter operated under different levels, THD Values are tabulated. Among all the levels total harmonic distortion is low for when the inverter is operated in five level mode and observe from the Figs. 24, 25 and 26, Every fifth harmonic element is removed. In comparison to the 2-level and

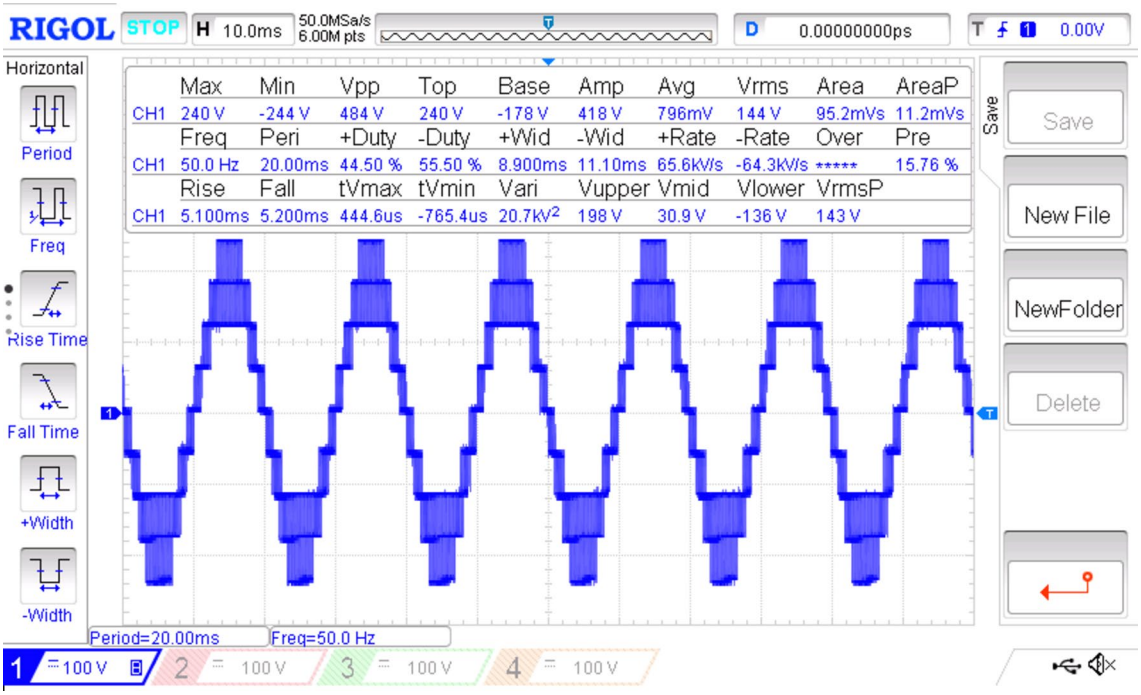

Figure 18. 5-φ 5-level line voltages (*Vac*) of proposed CHBML inverter.

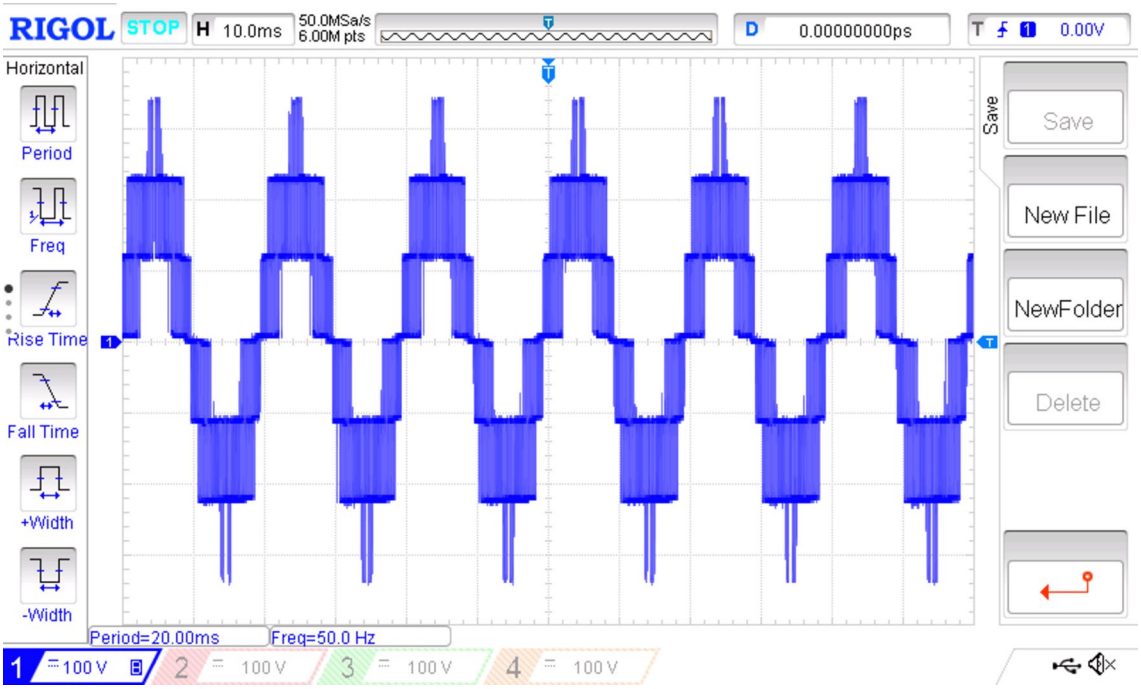

Figure 19. 5-φ 5-level line voltages (*Vac*) of proposed CHBML inverter.

3-level inverters, the proposed inverter operating in 3-level mode reduces overall harmonic distortion by 42% and 59%, respectively, when operating in 5-level mode.

For one phase leg switches, switching losses are also computed per unit, and Table 5 displays the total losses.

The proposed CHBML inverter fed to the FPIM, the speed is measured by using the speed sensors and by varying the frequency based on the set speed and hence the no. of levels is increased. From Figs. 27, 28, 29, 30 w.r.t the set speed, the levels are changed accordingly whenever the5-Level output is required the set speed fixed at 900 rpm.

3-Level output is obtained when the set speed is maintained as below 900 rpm. For 2-Level output only 5-legs are active out of 20 legs (or) 10 switches out of the 40 switches of the proposed inverter.

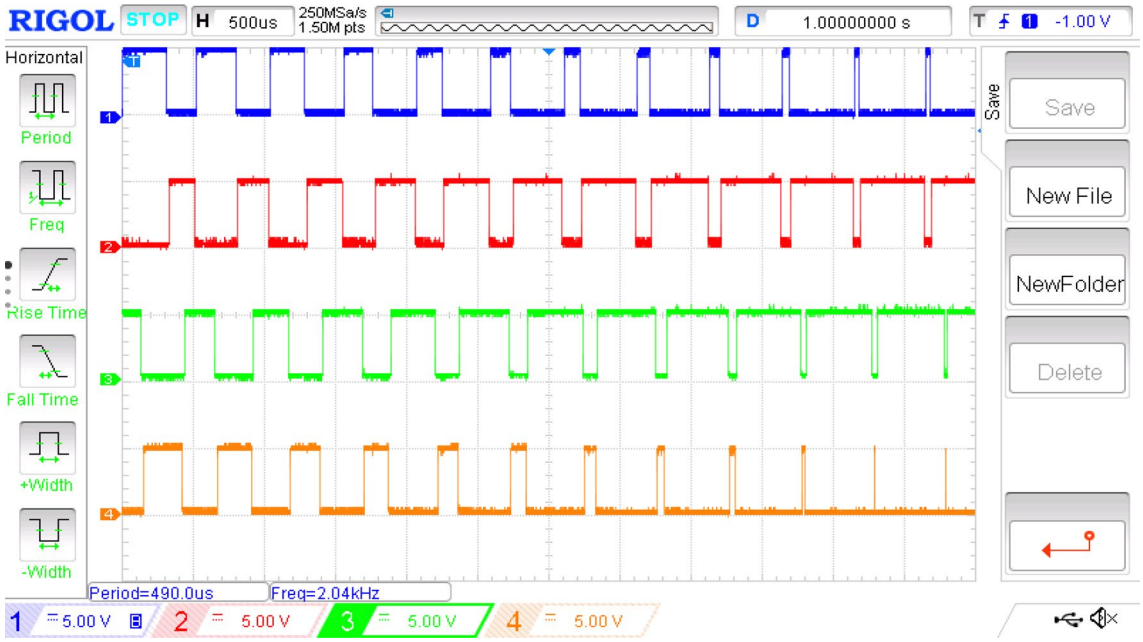

Figure 20. Pulses for each phase for upper leg switches.

Simulation and Experimental phase current results are shown from Figs. 31, 32, 33 w.r.t the set speed, the magnitude of the current will not be changed it is around 4A in all the cases.

FPIM operated at various speed corresponding current measured interms of the THD at various frequency conditions shown in from Figs. 34, 35, 36, 37. Measured THD values are Tabulated in Table 6.

The proposed induction motor Dynamic Response as shown in Figs. 38, 39, 40 for various conditions and tabulated in Table 7. From Table 7 the proposed induction motor takes the less time with 5-level CHBML inverter for Speed changes from one state to the other state compared to the lower levels of the Five leg Inverter operating modes.

Comparison of MLI topologies for five-phase induction motor drives

Induction motors with five phases present a strong substitute for applications that need precise control and great output. But in order to get greater efficiency and effectiveness out of these motors, choosing the best inverter architecture is essential. A promising possibility that is being investigated in this work is a CHB-MLI with IPD PWM control. This section explores the main benefits of the suggested CHB-MLI approach over other popular MLI topologies, such as NPC and FC MLIs. By emphasizing these advantages, to show that CHB-MLI is a good choice for five-phase induction motor driving, especially in the following scenarios:

- *Reduced THD* Without additional optimization, the suggested CHB-MLI with IPD PWM control technique yields a THD of 20.71%, which may be less than previous MLI topologies. This may help lower heating and increase motor efficiency.
- *Simpler control* The modular design of CHB-MLI, combined with independent H-Bridge control, allows for simpler control. This can be useful for real-time implementation, particularly if the suggested system makes use of an FPGA controller.
- *Cost-effective* Because CHB-MLI uses conventional switches instead of FC-MLI and NPC-MLI, which call for extra flying capacitors or clamping diodes, it may be less expensive. This is especially helpful for five-phase systems with an increasing number of switches.

The advantages of the suggested system are illustrated by the following comparison of the suggested CHB-MLI with two other widely used MLI topologies Table 8.

Conclusion

An experimental investigation was carried out for a low cost FPGA based five level CHBMLI fed FPIM Drive. The proposed CHBMLI finds the major solution for the thrust of power quality issues. In this proposed topology, desired output voltage and power levels are obtained by using high power ratings with voltage limited power semi conductor devices. In the instance of the suggested supply, the torque ripple content and frequency are 0.05 Vp and 10 f, compared to 0.134 Vp and 6 f in the standard 3-φ supply. The proposed drive efficiently operated with different levels without interrupting the dynamic performance of the drive. By observing the switching losses, the ripple content reduced by 37% by using proposed multi-phase supply. THD content in 1-φ supply is 48%, 3-φ supply is 31%, 5-φ supply 21%, thus 56% can be reduced compared to 1-φ, 32% can be reduced compared to 3-φ. Simulation results were carried out using V/f speed control method and the results were validated using

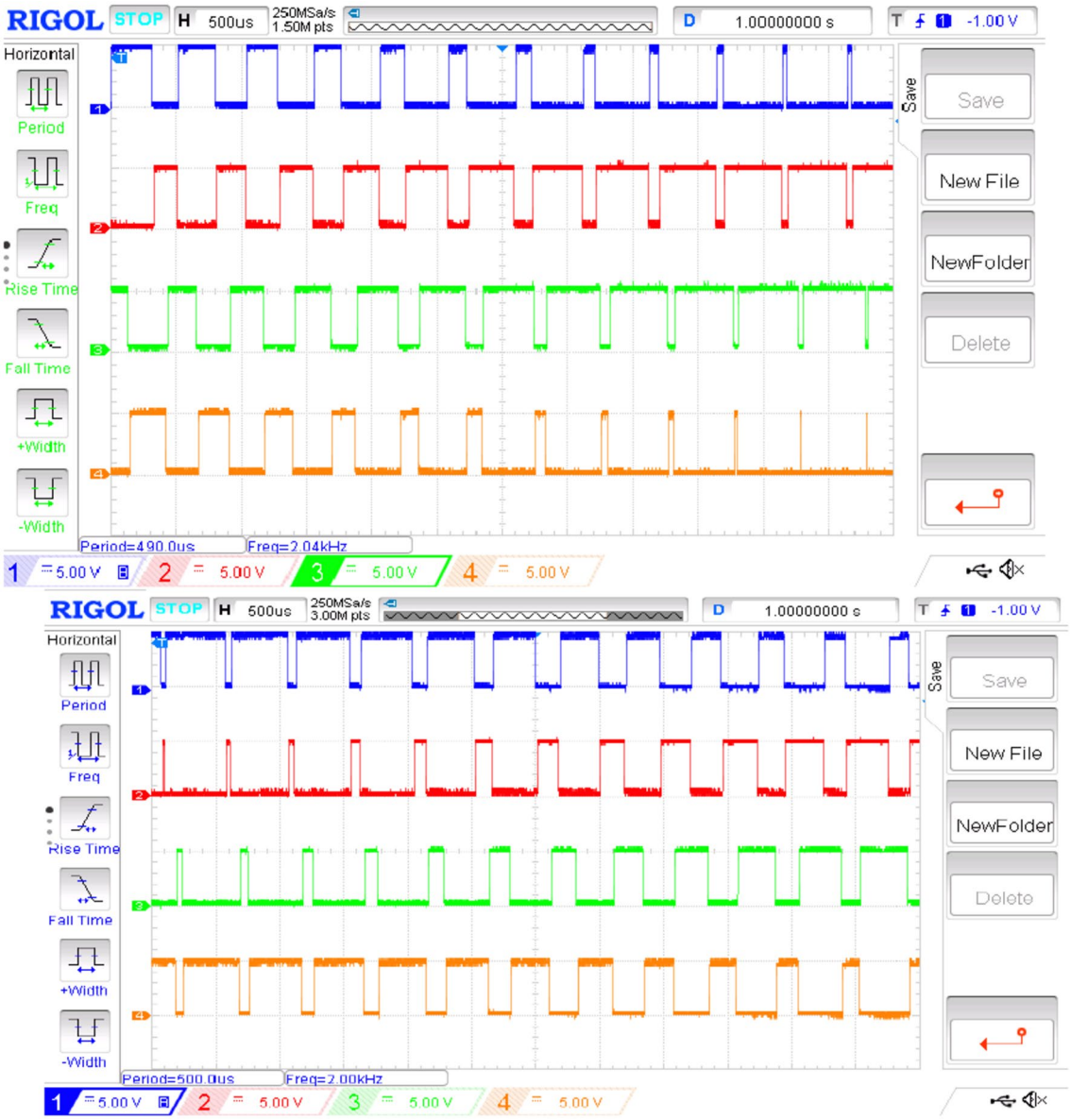

Figure 21. Pulses for lower leg switches for each phase.

proto type module under variable speed mode. THD has been compared using harmonic spectrum analysis. It reduces the cost of the filter designing components. Higher order harmonics are easily eliminated by means of filters. By utilizing the proposed drive the revolving magnetic field is maintained constant, like electric hybrid vehicles, traction, and electric ship propulsion, aircraft's etc.

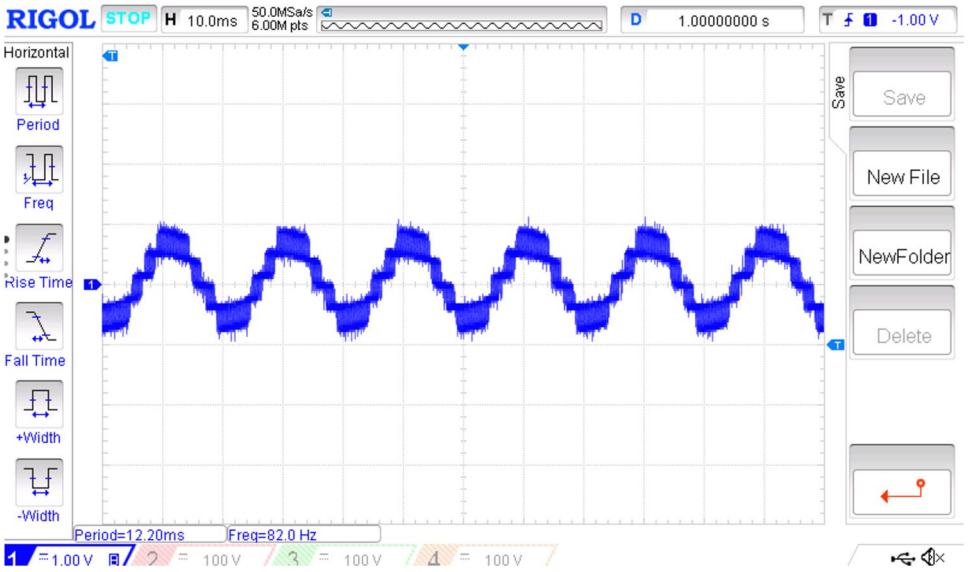

Figure 22. Phase currents with R-load.

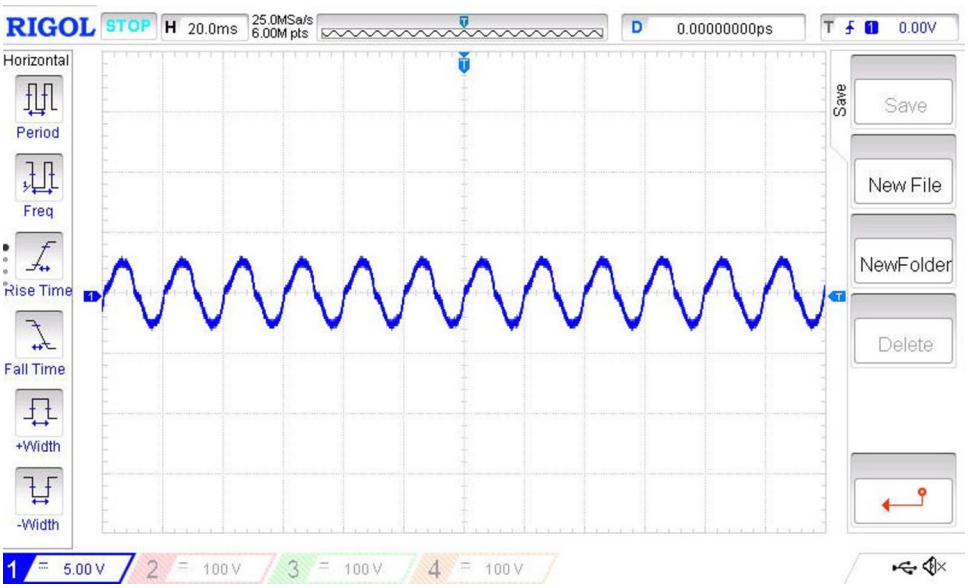

Figure 23. Phase currents with motor as a load.

Levels of proposed inverter	THD (%)
2-Level	17.7
3-Level	10.3
5-Level	7.3

Table 4. THD of proposed CHBML inverter.

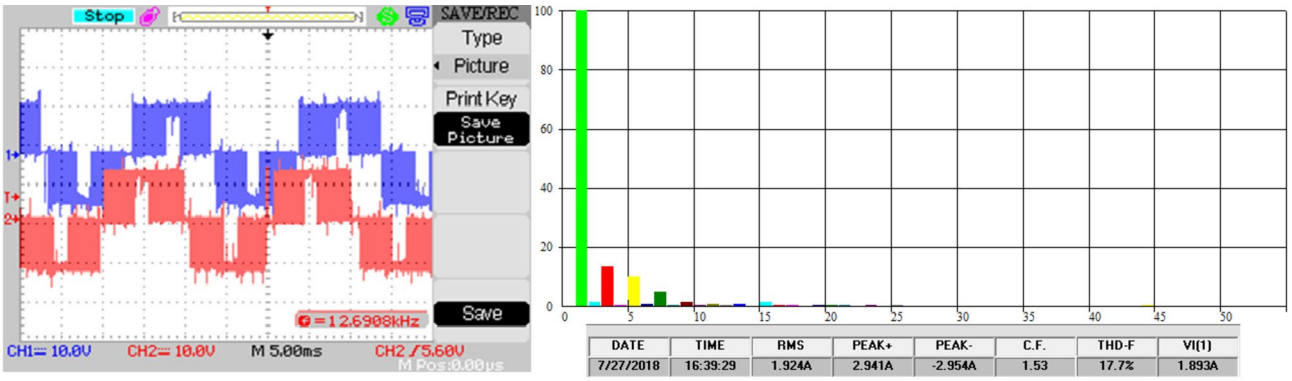

Figure 24. Phase voltages of proposed CHBM inverter for 2-level.

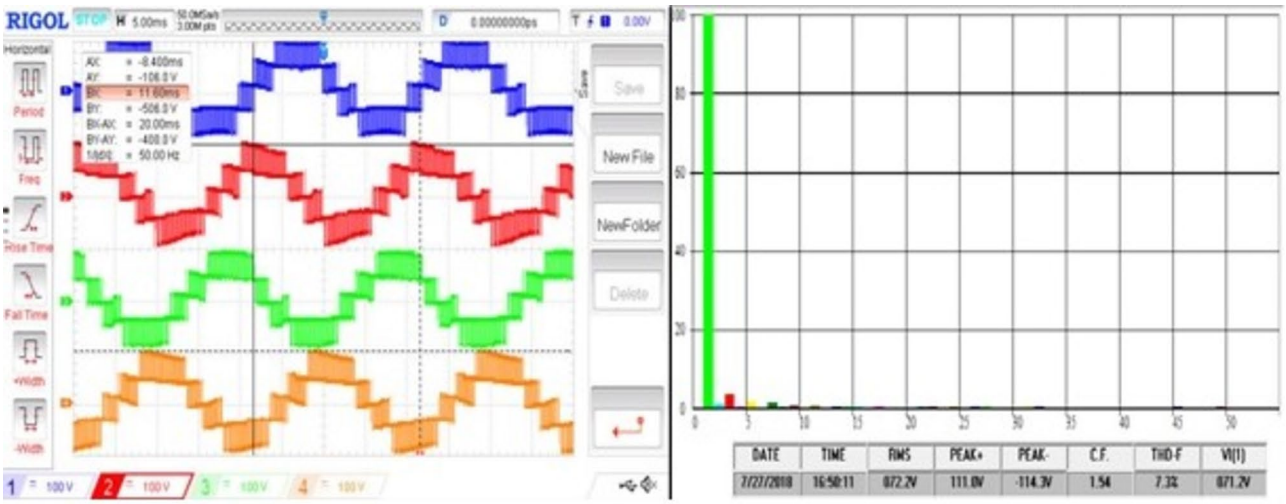

Figure 25. Phase voltages of proposed CHBM inverter for 3-level.

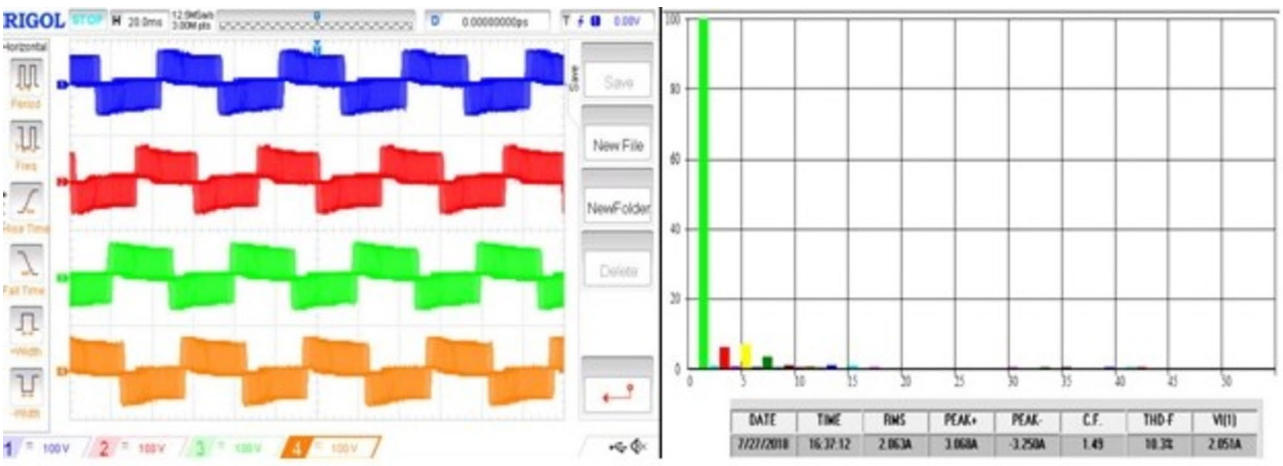

Figure 26. Phase voltages of proposed CHBM inverter for 5-level.

Switches	P.U switching losses
S_1 (S_2) and S_3 (S_4)	0.0033
S_1^1 (S_2^1) and S_3^1 (S_4^1)	0.0054
Total losses	0.0174

Table 5. Switching losses.

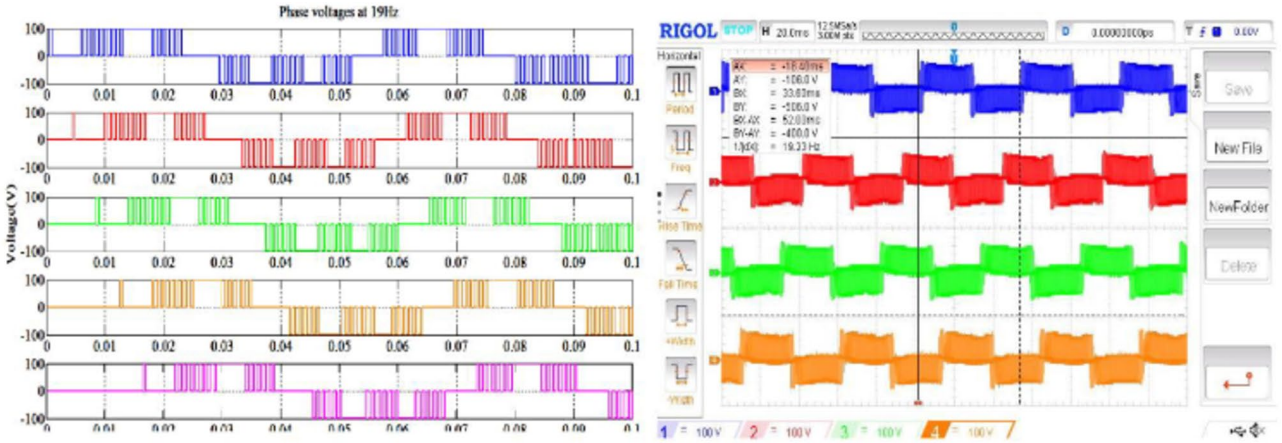

Figure 27. Simulation and experimental 5-φ 3-level at 19 Hz with speed 570 rpm.

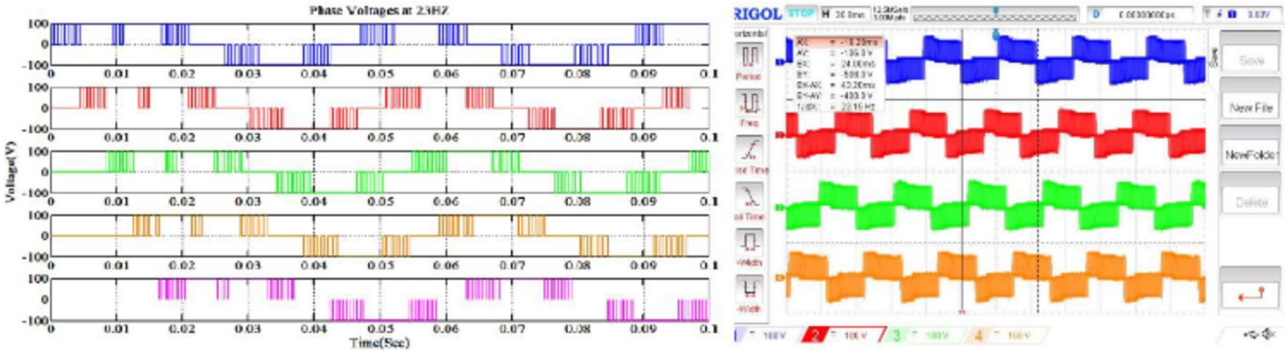

Figure 28. Simulation and experimental 5-φ 3-level at 23 Hz with speed 690 rpm.

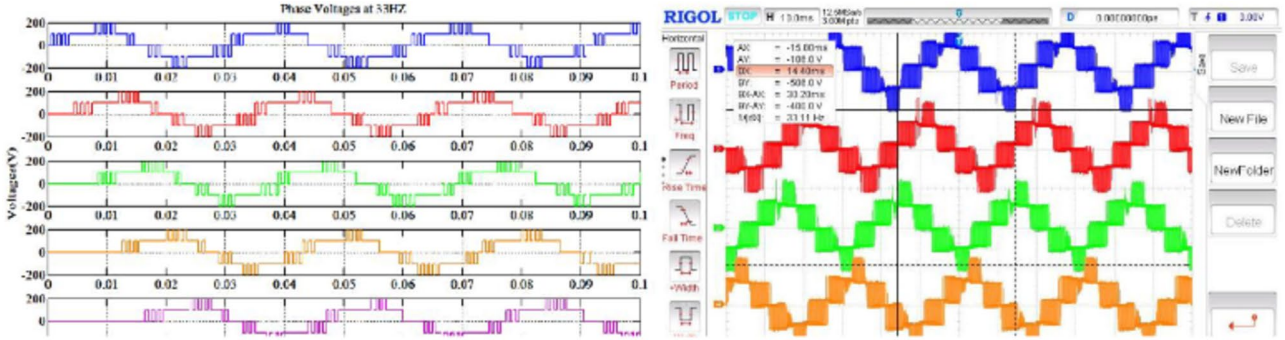

Figure 29. Simulation and experimental 5-φ 5-level at 33 Hz with speed 990 rpm.

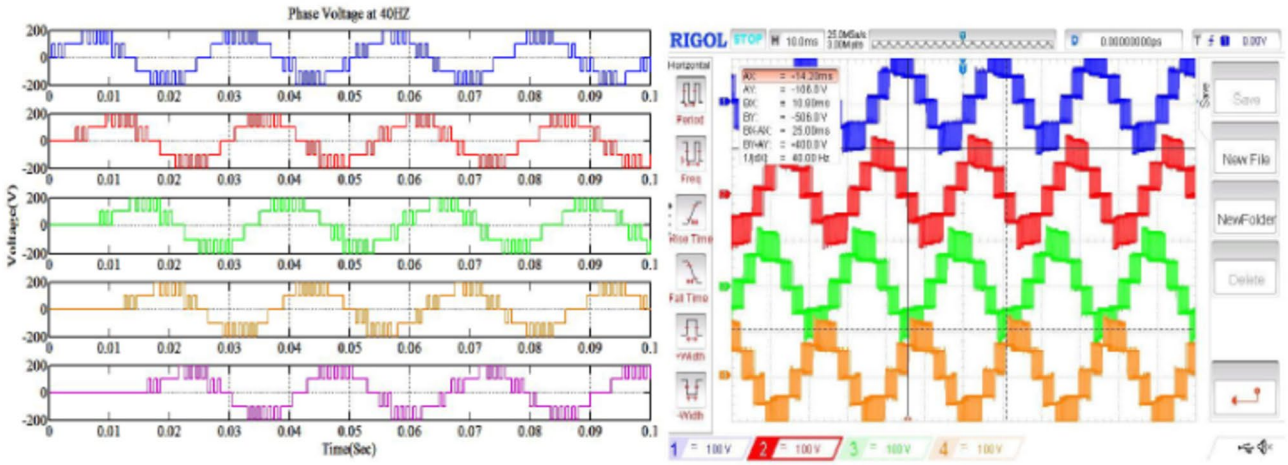

Figure 30. Simulation and Experimental 5-φ 5-level at 40 Hz with speed 1200 rpm.

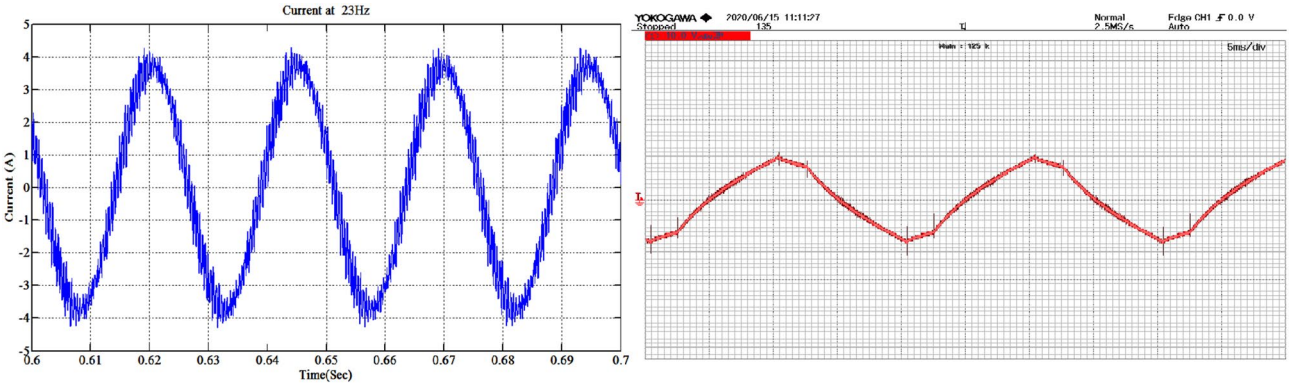

Figure 31. Simulation and experimental 5-φ motor current at 23 Hz with speed 690 rpm.

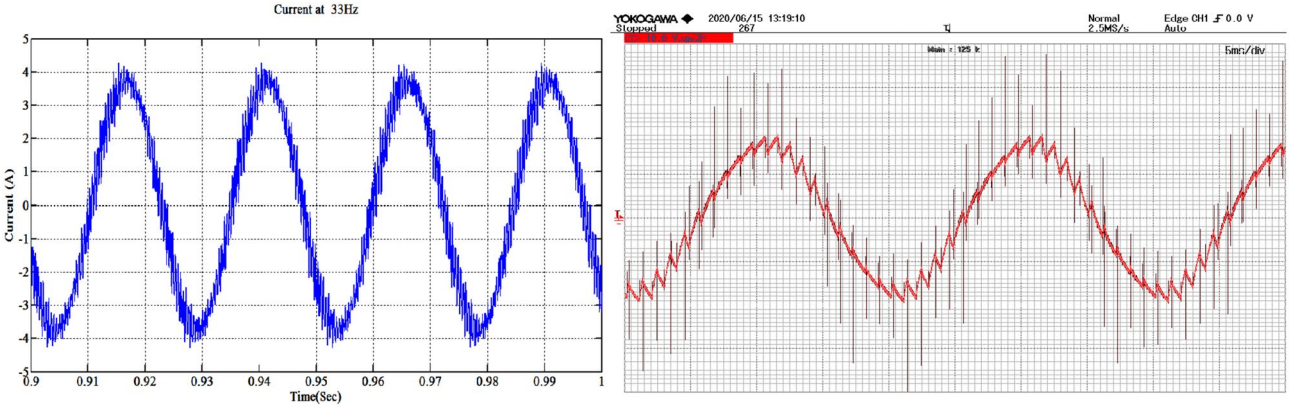

Figure 32. Simulation and experimental 5-φ motor current at 33 Hz with speed 990 rpm.

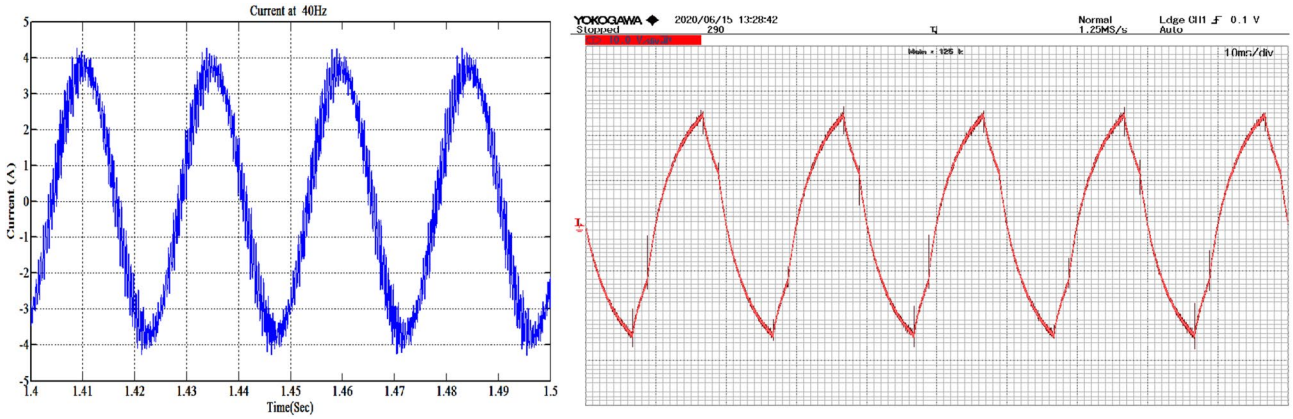

Figure 33. Simulation and experimental 5-φ motor current at 40 Hz with speed 1200 rpm.

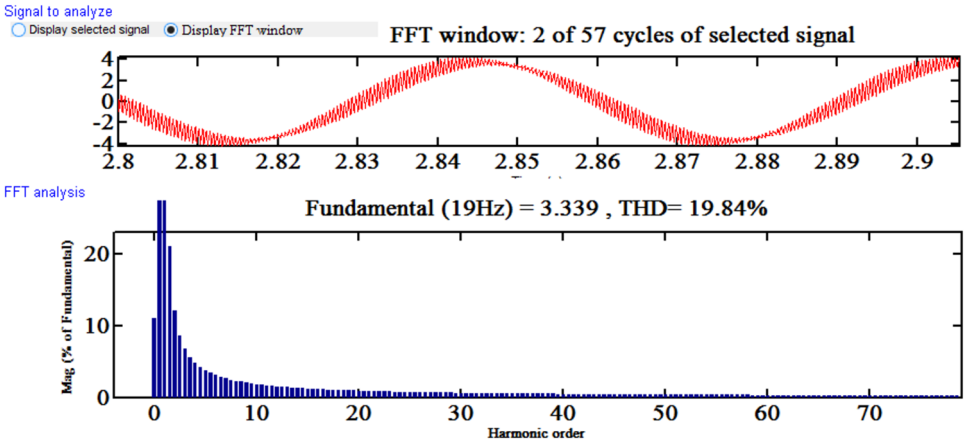

Figure 34. FPIM phase current THD at 19 Hz.

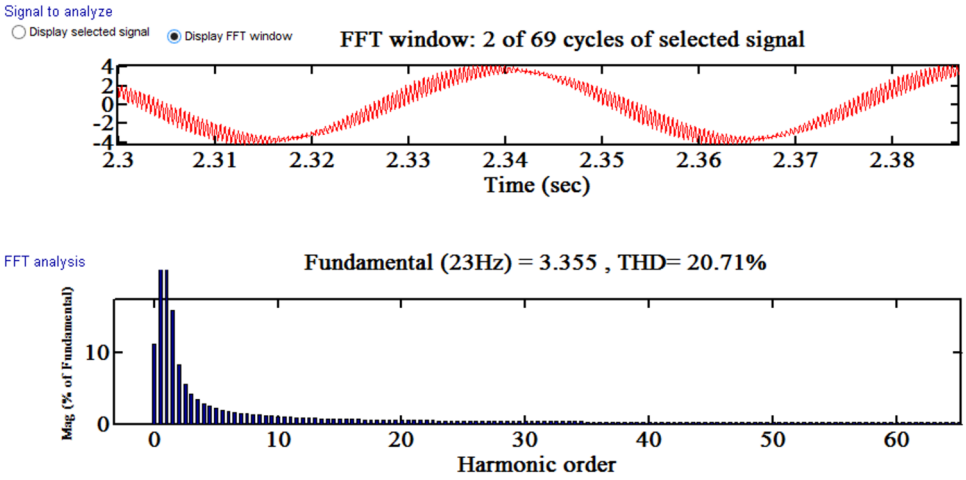

Figure 35. FPIM phase current THD at 23 Hz.

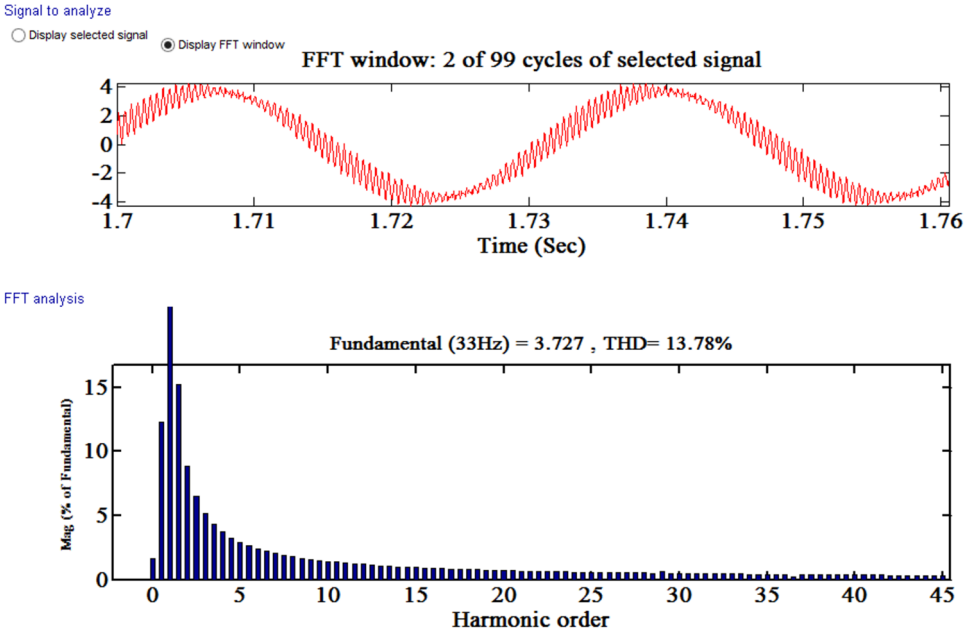

Figure 36. FPIM phase current THD at 33 Hz.

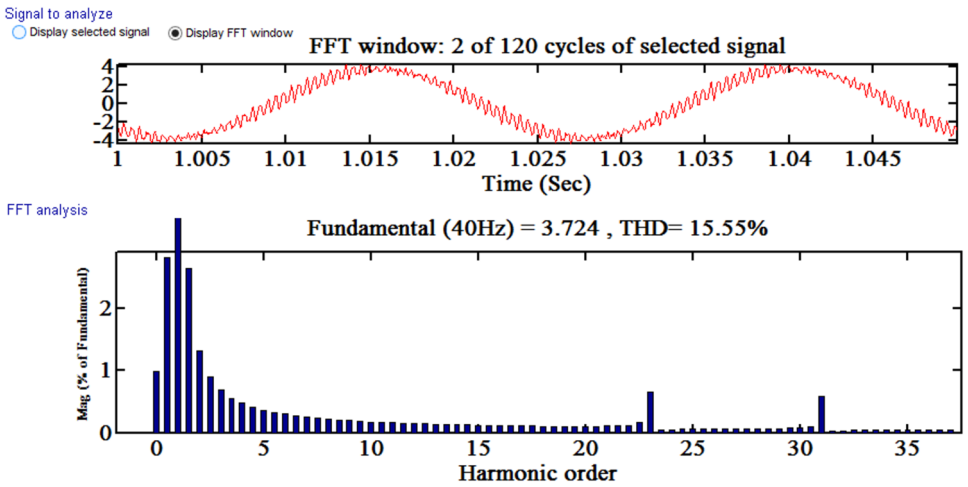

Figure 37. FPIM phase current THD at 40 Hz.

Motor current at various frequencies	% THD
19 Hz	19.84
23 Hz	20.71
33 Hz	13.75
40 Hz	15.58

Table 6. THD of proposed CHBML inverter.

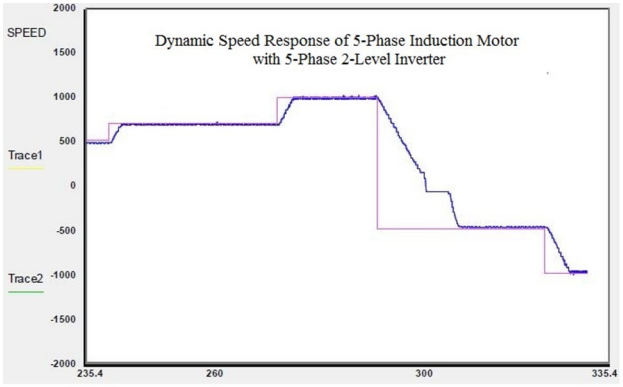

Figure 38. Dynamic speed response of proposed CHBM inverter for 2-level.

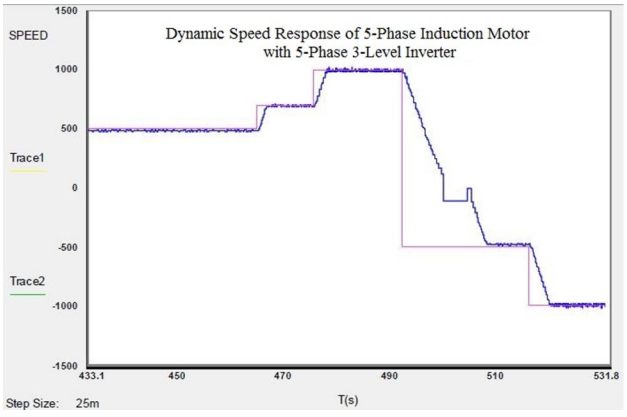

Figure 39. Dynamic speed response of proposed CHBM inverter for 3-level.

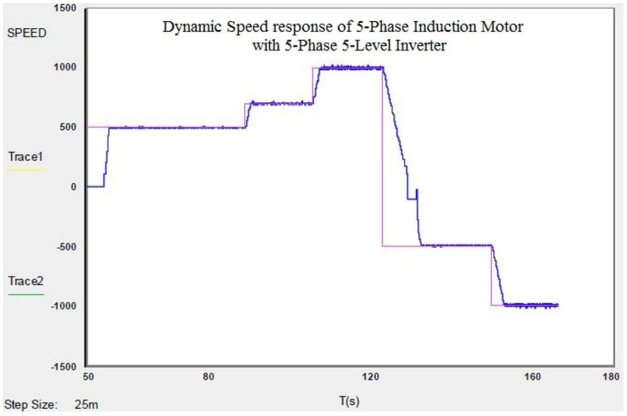

Figure 40. Dynamic speed response of proposed CHBM inverter for 5-level.

Levels of proposed inverter	500 to 700	700 to 1000 s	1000 to -500	-500 to -1000
2-Level	2.5 s	3.6 s	16.4 s	4.8 s
3-Level	2.1 s	2.5 s	15.2 s	4.2 s
5-Level	1.5 s	1.9 s	9.8 s	3.2 s

Table 7. Step change in speed (rpm).

Features	CHB	FC	NPC/DC
Structure	Simple and modular, uses separate DC sources for each H-bridge	Complex circuit with multiple flying capacitors for voltage balancing	Complex circuit with clamping diodes for voltage balancing
Control complexity	Less complex due to independent H-bridge control	More complex due to flying capacitor voltage balancing	More complex due to clamping diode voltage balancing
Component cost	Lower cost switches as only requires standard switches	Higher cost due to flying capacitors	Higher cost due to additional clamping diodes
THD (%)	20.71	50.56	39.72
Target application	Suitable for high power applications due to modularity	Suitable for medium power applications	Suitable for medium power applications

Table 8. Comparison of MLI topologies for five-phase induction motor drives.

Data availability

The datasets used during the current study are available from the corresponding author on reasonable request.

Received: 11 April 2024; Accepted: 26 July 2024
Published online: 22 August 2024

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Acknowledgements
The authors extend their appreciation Chonnam National University (Grant number: 2024-0926) and to King Saud University (KSU) for funding this work through the Re-searchers Supporting Project Number: (RSP2024R387).

Author contributions
All authors contributed equally to the conceptualization, formal analysis, investigation, methodology, and writing and editing of the original draft. All authors have read and agreed to the published version of the manuscript.

Funding
This study was financially supported by Chonnam National University (Grant number: 2024-0926) and by King Saud University through the Researchers Supporting Project Number: (RSP2024R387).

Competing interests
The authors declare no competing interests.

Additional information
Supplementary Information The online version contains supplementary material available at https://doi.org/10.1038/s41598-024-68713-z.

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